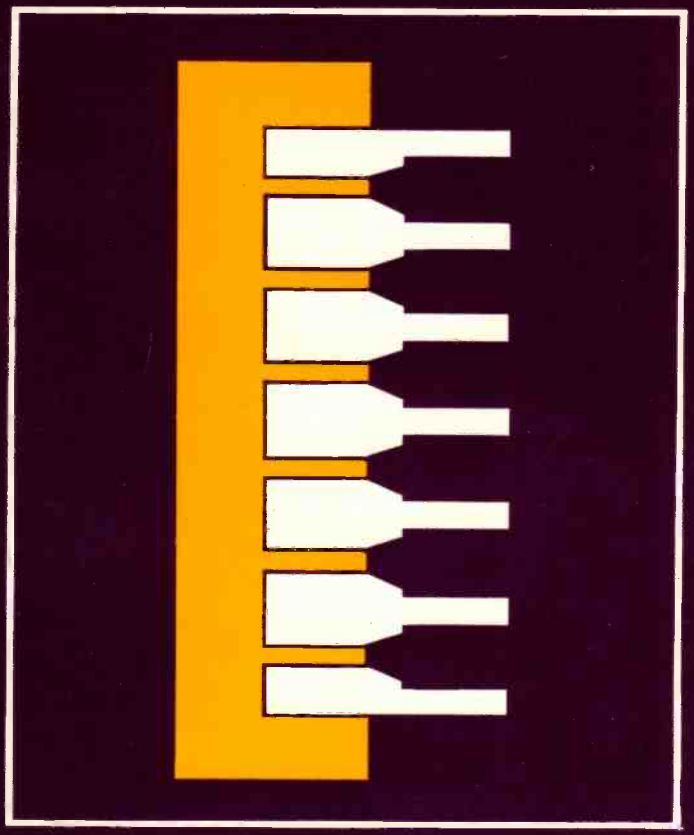
Second Book of CMOS IC Projects

R.A. PENFOLD



SECOND BOOK OF CMOS IC PROJECTS

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by
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Chapter 1

INTRODUCTION TO CMOS DEVICES

Most digital I.C. families contain devices which can be used in analogue applications, and a feature of CMOS devices is that they work extremely well in many analogue applications. They are somewhat better in this respect than other logic families; they also have certain other advantages, as will be explained shortly, and CMOS devices are probably the most versatile and useful range currently available.

It was in the early 1970s that CMOS I.C.s were first introduced, but they were not widely used at first because they were comparatively expensive, and had the reputation of being difficult to use and unreliable. Current CMOS devices have been much improved and have also fallen in price to the point where they are now amongst the cheapest available. This has led to their gradual acceptance in electronic designs for the amateur, and they have now achieved a high degree of popularity.

The book '50 CMOS I.C. Projects' (by the same author and publisher) covers a very wide range of project types, but by no means covers all the possible uses of CMOS devices.

The aim of this second book is to provide a further selection of useful circuits, mainly of a fairly simple nature, and therefore within the capabilities of both the beginner and more advanced constructor. The contents of this second book have been selected to produce a minimum of overlap between the two, and the versatility of CMOS devices is such that there is no problem in achieving this.

CMOS Basics

There are two main features which distinguish CMOS devices from those in other logic families. They have a low static

current consumption (usually only a fraction of a microamp) and they have an exceptionally high input impedance of typically about 1,000,000 Meg. ohms. This is achieved by the use of Complementary MOS transistor (CMOS) circuitry.

This type of circuitry and these two basic characteristics are most easily explained by considering the circuit of a basic CMOS inverter, and this is given in Fig. 1(a). The two transistors are MOS (Metal Oxide Semiconductor) or IGFET (Insulated Gate Field Effect Transistor) devices as they are alternatively known. They are not depletion type F.E.T.s such as those commonly employed in H.F. and V.H.F. applications but are of the enhancement type. A depletion device normally conducts quite heavily and can be switched off by means of a reverse bias to the gate terminal. An enhancement device is just the opposite of this, and will be switched off unless it is supplied with a forward gate bias. In this respect an enhancement F.E.T. is rather like an ordinary bipolar transistor, but there is the important difference that it is voltage and not current operated. In other words it is the gate voltage that determines whether the device conducts or not, and not the amount of current that flows into the gate. The gate current is negligible anyway as MOSFET devices have extremely high input impedances. For most practical purposes they can be regarded as having an infinite input impedance.

The action of the circuit of Fig. 1(a) is very straightforward, and may already be apparent. With the input at logic 0 ('low' or about equal to the negative supply rail) the P channel device will be switched on and the N channel device will be turned off. The output will therefore be at logic 1 ('high' or about equal to the positive supply rail). Taking the input to logic 1 reverses the states of the two transistors with the N channel device being biased on and the P channel one becoming cut off. Thus the output alway assumes the opposite logic state to the input and the inverter action is produced.

Figs. 1(b) and 1(c) show the effective output circuit of a CMOS inverter in the low and high states respectively. Obviously in either case there will be no current flowing

through the output circuitry as in each case one switch is open, and will block any current flow.

It is possible to gain the impression from this explanation that CMOS devices consume no current whatever, but this is not the case. There is inevitably a small leakage current through whichever output device is turned off, although this

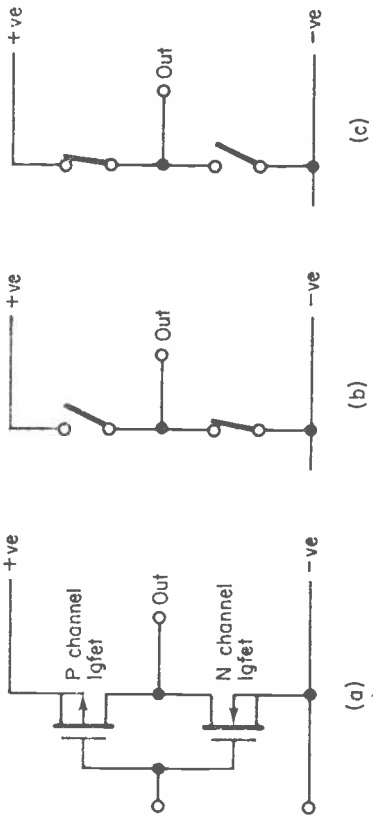


Fig. 1. (a) Basic CMOS inverter circuit. (b) The effective low output circuit. (c) The effective high output circuit.

will only be a small fraction of a microamp and will not normally be significant. However, a CMOS device will consume current as its output changes from one state to the other. This is because, in effect, one switch closes before the other one opens, and a conductive path is thus produced between the supply lines. This means that the current consumption of a CMOS device is largely dependent upon the frequency at which it is operating. At low audio frequencies the average current consumption would typically be only a few microamps, but at a frequency of a few MHz it would be several mA.

At high frequencies CMOS devices tend to lose the advantages of low supply current and high input impedance (the latter being reduced by stray input capacitances) and they are not normally used at frequencies beyond about 5 MHz. Many CMOS devices are not guaranteed to operate at frequencies beyond about 5 MHz anyway. These devices are mainly used in low and medium speed applications where they perform extremely well.

One drawback of CMOS devices is their relatively low output current capability. Although the MOS transistors used in CMOS devices have been described as analogous to switches, it would perhaps be more accurate to think of them as variable resistances. In the off state they have a resistance of thousands of Meg. ohms and this falls to a few hundred ohms in the on state. This 'on' resistance limits the transition supply current to a reasonable level, but it obviously also limits the output current to several mA.

However, this is not a major drawback as the output current capability is more than adequate to drive small loads such as L.E.D. indicators, and high current loads such as loudspeakers require output buffering regardless of what family of logic devices is utilised.

There are two other advantages of CMOS devices over other logic families which are worthy of mention. One is the fact that they are not restricted to the usual 5-volt supply, but will

operate over a very wide supply voltage range. Devices having an 'A' suffix will operate over a range of 3 to 15 volts (12 volts is the recommended maximum voltage), and the 'B' suffix devices which are gradually replacing the 'A' series devices will operate over a range of 3 to 18 volts (15 volts recommended maximum).

The other advantage is that CMOS I.C.s have high noise immunity and are not readily spuriously triggered by noise spikes on the supply lines.

Manufacturers

CMOS I.C.s are manufactured by several companies, and this has resulted in otherwise identical devices being available under slightly different type numbers. An R.C.A. quad 2 input NOR gate could have CD4001AE as its type number, where the Motorola direct equivalent of this could have MC14001CP as its type number, for example. Even devices from the same manufacturer and of the same basic type can have slightly different type numbers, the suffix being used to indicate such things as package type and operating voltage range.

However, in general, manufacturers all use the same basic type numbers (e.g. 4001 for a quad 2 input NOR gate) and normal retail outlets sell the 14 and 16 pin (as appropriate) DIL plastic package devices under the basic type numbers. Any device obtained through normal retail outlets should work perfectly well in the circuits provided in this book, and should conform to the leadout details provided at the end.

Protection

Many readers will be aware of the fact that manufacturers recommend that certain precautions should be taken when handling and using CMOS devices, and these are mainly due to the fact that these I.C.s can easily be damaged by high

voltage static charges. These charges are readily generated in modern environments.

Although all modern CMOS I.C.s incorporate protection circuits, they can still be damaged by static charges. CMOS devices are normally supplied in some form of protective packaging such as conductive foam (to short circuit any static build-up) or a plastic tube (to prevent any static charge from reaching the device). It is advisable to leave the device in the special packing until it is time to connect it into circuit, and then either use a socket or solder the device into circuit using a soldering iron with a properly earthed bit. CMOS I.C.s should be the last components that are wired into circuit. There are protective diodes in CMOS I.C.s which will produce a virtual short circuit across the supply lines if the supply polarity is incorrect. Always make sure the supply polarity is correct, and that the device has the correct orientation (incorrect orientation will result in the device being connected with the wrong supply polarity).

There are other recommendations such as using an earthed metal worktop, and never plugging a device into circuit while the power is switched on. This all tends to give an impression of CMOS I.C.s being extremely frail and impractical devices. The experience of the author and others with these devices does not bear this out, and treating them like any other device is unlikely to result in any failures. However, it should be borne in mind that ignoring the handling precautions probably nullifies any guarantee.

General

DIL plastic package CMOS I.C.s will operate over the wide temperature range of −40 to +85 degrees Centigrade (−55 to +125 degrees Centigrade for ceramic and flatpack versions). Even though these devices have a comparatively limited output drive capability, because of their extremely high input impedances they have a high fan out of 50. This is really limited by the input capacitance of the devices, and a much higher fan

out should be possible in low speed applications. An advantage of the fairly low maximum output current of these devices is that accidentally short circuiting an output to one or other of the supply lines is unlikely to result in any damage to the circuit since the output current will be limited to a safe level by the resistance of whichever output transistor is turned on.

Although with many logic families it is quite in order to simply ignore any unused inputs, this is not the case with CMOS I.C.s. Apart from leaving the input vulnerable to damage by static charges, stray signals such as mains hum may well cause the input to be switched from one logic state to the other. This will result in increased current consumption and could even result in a circuit malfunction in certain cases. Outputs are, of course, at a low impedance and when unused can simply be ignored.

Inverters

Many of the circuits that are featured in the following pages are based on the 4001 quad 2 input NOR gate. However, in most instances the two inputs of the gate are simply connected in parallel so that the device functions as a simple inverter. This is generally cheaper than using a device such as the 4069 hex inverter, but a proper inverter can be used if desired. It is also possible to use any CMOS NOR or NAND gate with its inputs connected in parallel so that it operates as an inverter. Note however, that in a few cases one or more sections of the 4001 are used as gates rather than as inverters, and in these cases only the 4001 can be employed. Where appropriate this is always made clear in the text and on the relevant circuit diagrams.

Chapter 2

MULTIVIBRATOR PROJECTS

The three types of multivibrator (bistable, monostable and astable) can all be readily produced using a 4001 device, and this chapter details a number of projects using the 4001 in these three modes.

Bistable Sequence Switch

A bistable circuit is easily produced from a couple of CMOS inverters simply by cross coupling the inputs and outputs via resistors. Fig. 2 shows a basic CMOS bistable which has been provided with a small amount of additional circuitry so that it operates as a sequential switch. This type of circuit causes a load to be successively switched on and off each time a push button switch is momentarily operated.

R3 and R4 are the two cross coupling resistors. When power is initially applied to the circuit one inverter assumes the low output state and the other takes up the high output state. Under normal circumstances, which inverter assumes which output state is determined by a number of factors such as stray capacitances and the individual propagation delays of the two gates. In this case though, C2 has been included so that the switch-on states are predictable.

When power is applied to the circuit, the input of inverter 1 will be held at the negative supply rail potential by uncharged capacitor C2. The output of inverter 1 therefore goes high, and due to the coupling through R4 it takes inverter 2 input high as well. The output of inverter 2 goes low, and the coupling through R3 holds inverter 1 input low. This causes the circuit to latch with the output of inverter 2 low, Tr1 cutoff, and no power supplied to the load apart from insignificant leakage currents.

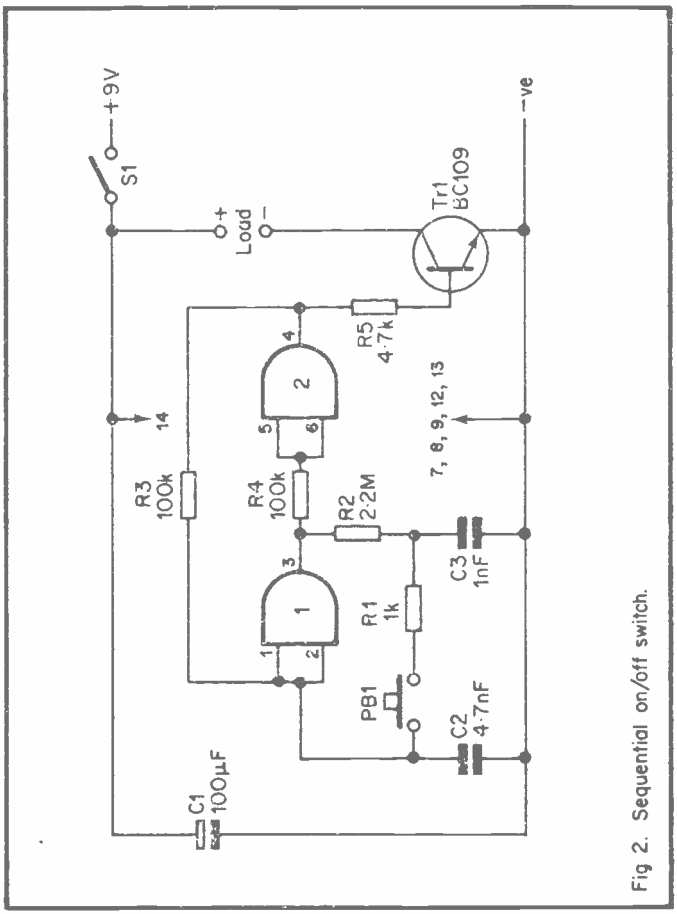


Fig 2. Sequential on/off switch.

As the output of inverter 1 is high, C3 will charge up via R2 to a voltage virtually equal to the positive supply rail potential. If PB1 is momentarily depressed, the input of inverter 1 will be connected to C3 via R1, and this will obviously result in the input going high. This drives inverter 1 output and inverter 2 input low, and causes inverter 2 output to go high. Even when PB1 has been released, the circuit will remain in the new state as the coupling through R3 will hold the input of inverter 1

high, and cause the circuit to latch. Tr1 will now be biased hard on by way of current limiting resistor R5, and power will be supplied to the load.

The output of inverter 1 is now low, and with PB1 open there is no path via R3 and R1 to the high output of inverter 2 to keep C3 charged up. It will therefore quite quickly discharge through R2 into the output circuitry of inverter 1.

If PB1 is once again operated, the input of inverter 1 will be taken low as it will be connected to the discharged C3 through R1. This will cause the bistable to be triggered back to its original state and it will latch in this state. With Tr1 now once again cut off, the load will receive no significant current.

With the circuit back in its original state, if PB1 is now operated the circuit will behave exactly as it did when PB1 was first depressed. Thus the load can be switched on and off by successive operations of PB1.

In the off state the circuit consumes negligible current, and in the on state only a little in excess of 1 mA. This is the base current for Tr1. The load should consume a maximum current of no more than 100 mA which is the maximum the BC109 can handle. Greater loads can be handled if a Darlington pair power transistor is used at the output (or two discrete devices connected to form a Darlington power device). If a relay or other highly inductive load is used, connect a protective diode (a 1N4002) in parallel with the load. The cathode (+) terminal of the diode must connect to the positive supply rail.

Sequential Touch Switch

The circuit diagram of the sequential touch switch is shown in Fig. 3, and this is basically the same as the previous circuit. The only differences are that PB1 and R1 have been replaced by touch contacts, and R3 has been raised in value so that the circuit is much more sensitive. This enables the circuit to operate with a fairly high switching impedance between C3

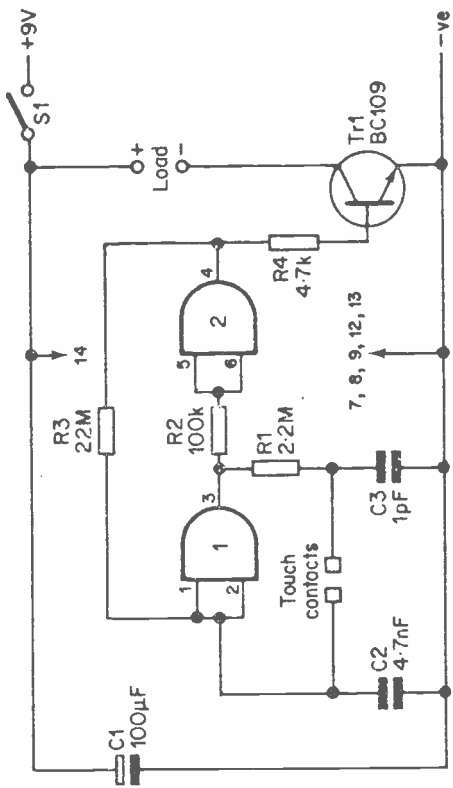


Fig. 3. Sequential touch on/off switch.

and the input of inverter 1. In fact, even if the skin resistance of the operator's finger is several Meg. ohms, if this bridges the touch contacts it will be sufficient to take inverter 1 input to the same logic state as the junction of R1 and C3, and thus trigger the circuit to its alternative state.

The notes on the circuit of Fig. 2 also apply to this circuit. In addition, it is perhaps worth mentioning that if the 22 Meg.

ohm resistor for the R3 position proves to be difficult to obtain, two 10 Meg. ohm components wired in series can be used instead. The touch contacts can be any two small areas of metal which are closely spaced but well insulated from one another. These are often made from copper laminate (p.c.b. material) or a couple of panhead screws mounted side by side on an insulating panel. With a little ingenuity it should not be too difficult to fabricate suitable contacts. For best long term reliability the contacts should be made of a metal that does not easily corrode.

If the finished unit does not always trigger reliably from one state to the other when the touch contacts are operated, adding a 10 nF capacitor in parallel with R3 should cure the problem. If the circuit still seems to be unreliable then this probably means that the touch contacts are inadequate.

Basic Burglar Alarm

The ability of a bistable multivibrator to act as a latch can be used to good effect in burglar alarm circuits. Most burglar alarm circuits are very simple, but despite this they are amongst the most useful and popular of all electronic projects.

The majority of alarms are simple switch operated types, and are operated by switches which are fitted to the doors and windows which are to be protected. Most of the work in installing an alarm system is in the fitting and wiring up of these switches, rather than in the basic circuit.

There are two normal types of switch which can be fitted to the doors and windows; micro switches and reed switches. The former are just a form of mechanical switch which are designed to be operated automatically by something (obviously the doors and windows in this case) rather than manually. Reed switches consist of two metal reeds which are contained in a glass envelope. The two reeds are positioned parallel to one another with their ends slightly overlapping, but slightly spaced apart. If a magnet is brought close to the reeds they

become magnetised, and if the field is strong enough the mutual attraction between the two reeds draws them together so that they make mechanical and electrical contact. When the magnetic field is removed the reeds are no longer magnetised and their elasticity causes them to spring apart.

Reed switches are probably the easier type of switch to instal and the more reliable of the two, but not everyone would agree with this. Micro and reed switches can be obtained from some component retailers, and types specifically designed for use in burglar alarm systems are also available.

The switches can be arranged so that they are normally open (N.O.) and trigger the alarm by closing when a window or door is opened, but normally closed (N.C.) switches are more popular. These open when a door or window is opened, and activate the alarm. This type of switch is more easily installed as it requires less connecting wire than a N.O. system, and it also provides better security.

Another form of triggering switch is the pressure mat type. This consists of a mat to which two electrical contacts are made. Normally there is an open circuit between the two contacts, but if anyone steps onto the mat a short circuit is produced between the contacts. A few pressure mats strategically placed act as a good back-up to the door and window switches.

Since it is likely that a burglar alarm system will be used with both N.O. and N.C. switches, it must be designed accordingly. A basic burglar alarm circuit suitable for use with either type of switch is shown in Fig. 4.

When power is initially connected to the circuit, C2 will hold the input of the bistable in the low logic state, and so the output will also be in the low state. C2 will not be able to more than marginally charge up through R1 as inverter 1 input will be held at logic 1 by the coupling to the output of the bistable via the lower resistance of R3. Tr1 will therefore be switched off and the relay which forms it collector load will not be activated.

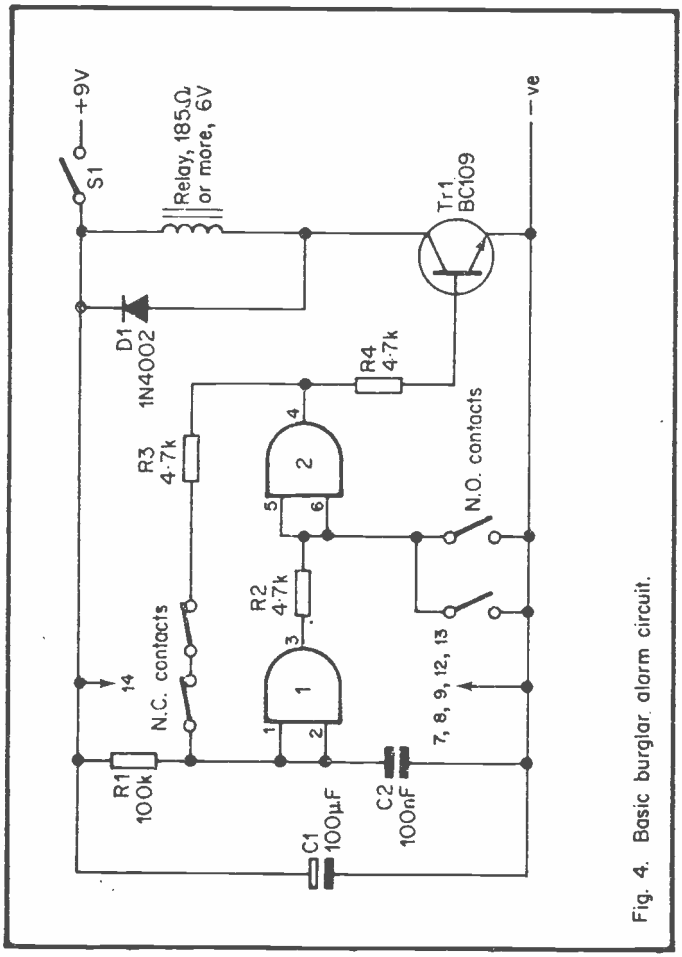


Fig. 4. Basic burglar alarm circuit.

If one of the N.C. contacts is opened, R3 will no longer hold inverter 1 input low and C2 will be free to charge up via R1. This it will rapidly do, and both the input and output of the bistable will go to logic 1. This results in Tr1 being biased on and the relay is energised. A pair of relay contacts are, of course, used to operate an alarm of some kind.

If the N.C. contact is now closed again, the bistable will not change state. The input and output are both in the high state, and the coupling through R3 simply reinforces this situation.

The circuit can also be triggered by closing one of the N.O. contacts. When the circuit is first switched on, both inverter 1 output and inverter 2 input will be at logic 1. If one of the N.O. contacts is closed it will take inverter 2 input low. This will cause the output of the bistable to go high and the relay to be energised. The coupling by way of R3 will take the input of the bistable high and cause inverter 1 output to go low. Even if the N.O. switch is now opened, the circuit will remain in its present state. The switch will not hold inverter 2 input low, but the coupling from the low output of inverter 1 via R2 will do so.

Thus, once the circuit has been triggered and the alarm is operating, the circuit will latch in that state, and the alarm cannot be silenced simply by returning the appropriate switch back to its original position.

D1 is a protective diode and quenches the high reverse voltage that would otherwise be generated as the relay de-energised. If not suppressed this voltage could easily damage one of the semiconductor devices in the circuit. C1 is a supply decoupling capacitor.

The quiescent current consumption should only be something in the region of 1 microamp, this being the total leakage current through C1, Tr1, and the CMOS I.C. This enables the unit to be economically powered from batteries, even though it will be left switched on for extended periods.

S1 is the on/off switch and should ideally be a key type.

Entry Delay

One problem with basic burglar alarm systems is that of re-entering the house once the alarm has been activated. One

way around this is to fit a key switch to a protected door so that the reed or micro switch can be disabled. If an N.C. switch is fitted to the door, the key switch should be wired in parallel with this, and will disable it when it is in the closed position. For a N.O. switch the key switch is wired in series with it, and will disable the N.O. contact when in the open position.

This system can be difficult to instal, and it is obviously undesirable to have an external switch that can partially disable the system, even if a concealed key switch is used. The normal way around this problem is to fit an entry delay facility to the circuit. This merely provides a short delay between the alarm being triggered and the alarm being sounded. The alarm circuit should be well concealed, built into a strong casing, and have a key switch to provide on/off switching. This enables the occupier of the premises to immediately go to the alarm and switch it off upon entry, but makes it unlikely that an intruder would be able to do so.

Fig. 5 shows how the circuit of Fig. 4 can be modified to provide an entry delay. Here a third inverter is used, and it is merely connected as a buffer at the output of the bistable. This means that the output of the buffer stage will be normally high, and so Tr1 has been replaced by a p.n.p. common emitter stage. This results in Tr1 being switched off under quiescent conditions, which is of course what is required.

When the circuit is triggered, the output of the bistable will go high and the output of the inverter will be driven low. However, C3 must be charged to about 50% of the supply voltage before the input voltage to the buffer stage will be sufficient to alter its output state. The values of R5 and C9 have been chosen to produce a delay of roughly 30 seconds before this does actually occur, and in this way the required entry delay is produced.

It is worth noting that C3 must be a good quality component as some low quality electrolytic capacitors have rather low leakage resistances, and would produce a greatly elongated

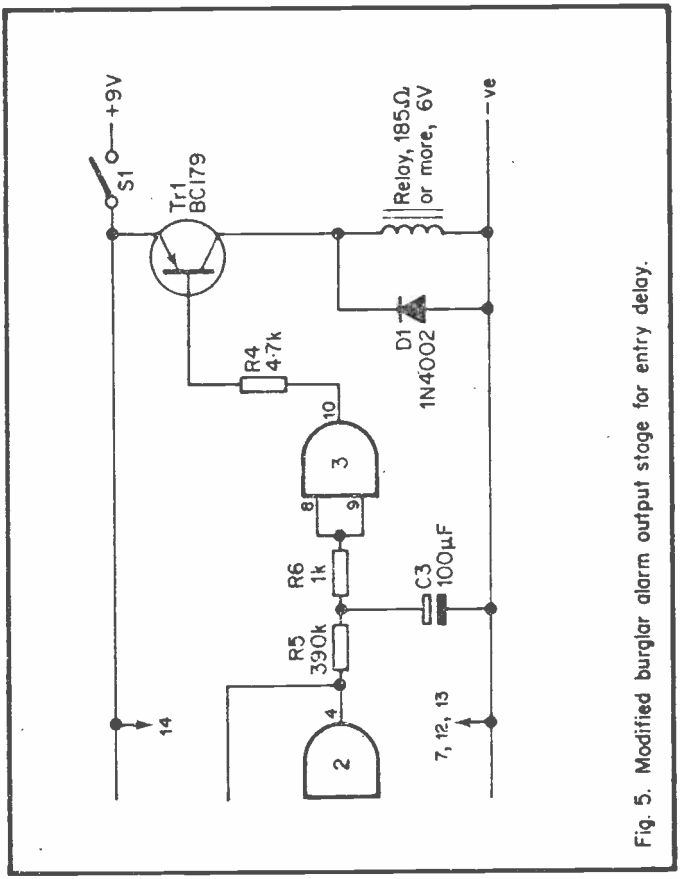


Fig. 5. Modified burglar alarm output stage for entry delay.

delay. In an extreme case the alarm could be prevented from sounding at all. The length of the delay can be altered to suit individual requirements by altering the value of R5. Increasing its value produces a proportional increase in the delay, and reducing its value has the opposite effect.

Exit Delay

Leaving the premises once the alarm has been switched on presents a similar problem to that of entry. It can be solved by fitting a disabling switch to one of the door switches, but a more satisfactory solution is to incorporate an exit delay into the alarm system. This merely consists of a small amount of additional circuitry which disables the alarm circuit for a pre-determined length of time after it has been switched on. This gives the occupier time to leave the premises before the circuit becomes effective.

The circuit of Fig. 6 shows how the basic alarm circuit of Fig. 4 can be modified to incorporate an exit delay facility. In the modified circuit inverter 2 is in fact used as a NOR gate rather than an inverter, and so only a 4001 device can be used in this circuit.

If either input 1 OR input 2 of a NOR gate is at logic 1, the output will be at logic 0. In the modified circuit, one input of gate 2 connects to a C – R timing network which consists of C3 and R6. This results in this input being held in the high state until the voltage at the junction of C3 and R6 falls below about 50% of the supply rail potential. The values of C3 and R6 have been chosen so that it takes approximately 30 seconds for the charge on C3 to reach a level where it takes the lower input of gate 2 to logic 0.

Until this does occur, the input state of the upper input of gate 2 is irrelevant with one input high the output must be low, regardless of the logic level of the other input. Thus, even if one or more of the sensor switches is activated, it will have no effect on the alarm.

Assuming that all the switches are in their proper quiescent states by the time the lower input of gate 2 goes low, the bistable will be in its normal standby state with the upper input at logic 1. Therefore, the output of the bistable will remain low and the alarm will not be activated.

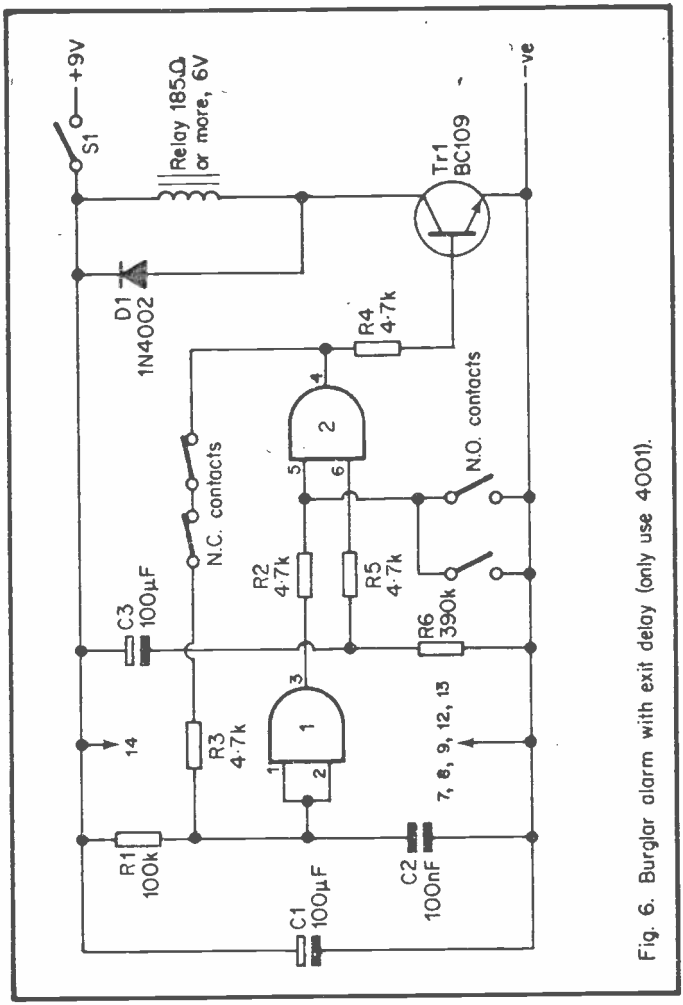


Fig. 6. Burglar alarm with exit delay (only use 4001).

However, if one of the sensor switches is now activated, the upper input of gate 2 will go low, and with both inputs low the output will go to logic 1 and sound the alarm. After the exit delay the circuit does in fact work normally, and once triggered it will latch in this state.

The notes on the timing components in the entry delay circuit of Fig. 5 also apply to the timing components of this circuit. Of course, if required, both the exit and entry delay modifications can be incorporated into the system.

Reaction Game

Logic I.C.s in general are well suited for use in various types of electronic games from simple designs using just a single I.C. to highly complex circuits using a multitude of sophisticated devices. The characteristics of CMOS I.C.s make them better suited to this general type of application than other logic families.

Complicated electronic games are beyond the scope of this book, but a simple reaction game circuit is provided in Fig. 7. This is designed for one player and consists of two basically identical circuits, each using a couple of CMOS inverters. Each pair of inverters is used in what is really a cross between a bistable multivibrator and an astable type.

Each bistable is formed by a pair of series connected inverters with D.C. positive feedback provided between output and input of the circuit by means of a resistor. One bistable is formed from inverters 1 and 2, and R2 as the feedback resistor. The other uses inverters 3 and 4 and has R5 as the feedback resistor.

A basic CMOS astable circuit is formed by wiring two inverters in series and biasing the first inverter to operate as a linear amplifier. This biasing is simply achieved by wiring a resistor between the input and output of the inverter, and a negative feedback action then biases the output to approximately half the supply voltage. To complete the astable a capacitor must be connected between the input and output of the circuit to provide a.c. positive feedback.

C2 and C3 provide the feedback paths for the astable circuits, and the necessary biasing is provided by R1 and R4. The

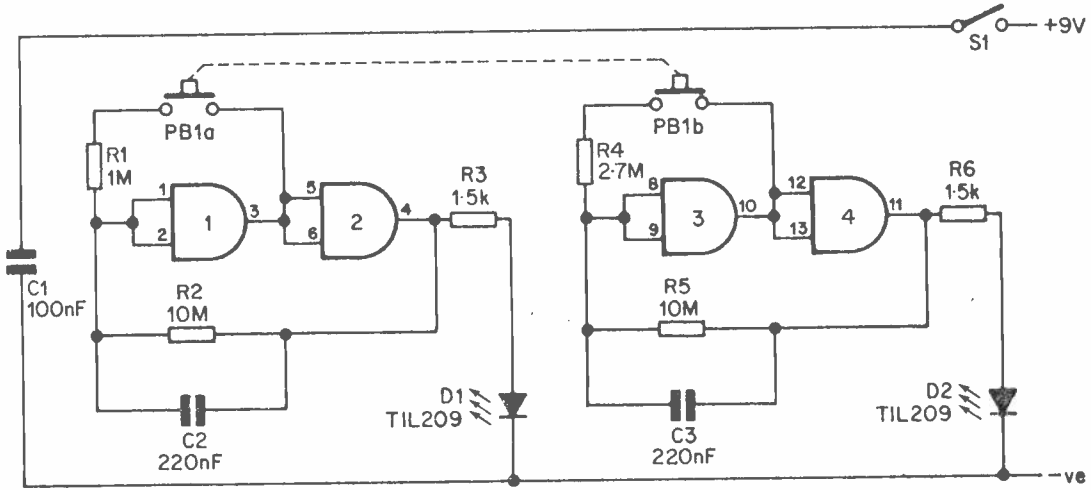


Fig. 7. Reaction testing game circuit.

circuit will only oscillate though when PB1 is depressed and the two bias circuits are completed. R2 and R5 have high values so that they will not block the operation of the astable by causing the circuit to latch. However, when PB1 is released and the biasing is removed from the circuit it will cease oscillating, and R2 plus R5 will then cause the circuit to latch. Each section of the circuit will latch in whatever state it happened to be in at the instant PB1 went open circuit.

A L.E.D. indicator is driven from the output of each bistable/astable circuit via a current limiting resistor (R3 and R6). Each L.E.D. will light up when the output it is driven from goes to logic 1. The component values have been chosen so that when oscillating, both circuits operate at only a very few Hz, and so the L.E.D.s can clearly be seen switching on and off. As R4 is higher in value than R1, the right hand astable operates at a lower frequency than the left hand.

The idea of the game is quite straightforward. The task is to press PB1 so that the L.E.D.s begin to flash on and off, and then release PB1 while both L.E.D.s are on. If this is achieved, as the circuits each latch in whatever state they were in when PB1 was released, both L.E.D.s should remain on.

This type of game is a lot more difficult than it sounds, and it is very difficult indeed to achieve a 100% success rate, or even something approaching this. A success rate of around 50% can easily be produced by sheer chance, and so a game should consist of ten or more attempts and not just one or two tries. The added difficulty of this game when compared to most others is that it is necessary to concentrate on two indicators, and not the more usual single indicator. Even with the two L.E.D.s placed close together this is difficult to do, and this adds a strong element of skill and co-ordination into the game.

The difficulty of the game can be altered by changing the speeds of the oscillators. Increasing the values of C2 and C3 will slow down the oscillators and decreasing these values will have the opposite effect. PB1 is a D.P.S.T. non-locking push button type, and although these are not as widely avail-

able as single pole types, they can be obtained from a few retail sources. Two single pole switches should not be used as this leaves the game open to cheating, but something like a D.P.S.T. sub-minature toggle switch will make a suitable alternative.

Sound Generator

Probably astable multivibrators are most widely used in various types of alarm to produce an audible signal. CMOS I.C.s are ideal for use in such applications as they make a good basis for very simple but highly effective alarm sound generators.

An audible alarm generator suitable for use in burglar alarm systems or similar applications is shown in Fig. 8. This is suitable for use with a nominal supply voltage of about 9 to 12 volts and with speakers having an impedance in the range 8 to 15 ohms. The output power is greatest when using a 12-volt supply and an 8-ohm speaker, the actual output power being about 4.5 watts. This falls to only about 1.8 watts when using a 15-ohm speaker and a 9-volt supply, but this is probably more powerful than most people would imagine, and will be capable of providing more than adequate volume for most purposes provided a reasonably efficient loudspeaker is used.

An audible alarm can simply consist of an astable circuit driving an output stage and loudspeaker. However, a single tone such as this, even if it is rich in harmonics, tends to be comparatively easily masked by other signals. Some form of modulated tone is usually more effective.

The circuit of Fig. 8 is a frequency modulated tone generator, and it has a nominal operating frequency of about 800 Hz. However, as the modulating frequency is a squarewave, it does not actually oscillate at this nominal frequency, and is switched between two frequencies a few hundred Hz either side of the nominal frequency.

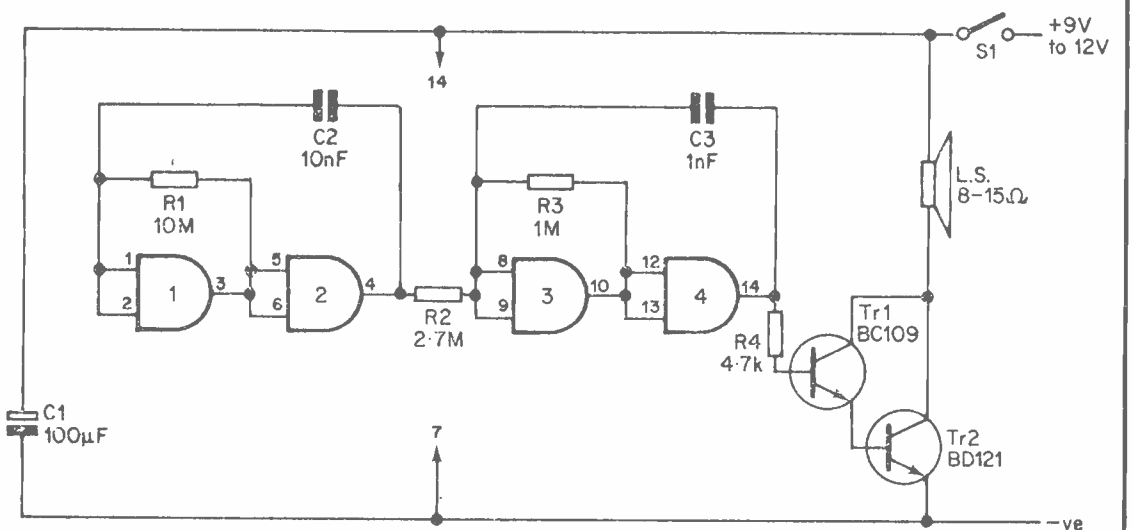


Fig. 8. Sound generator for burglar alarms, etc.

Inverters 3 and 4 are connected to form the tone generator which drives a Darlington pair output stage via R4. A Darlington pair is needed at the output in order to provide the fairly high output currents which will exceed 1 amp on peaks when using an 8-ohm speaker. For the same reason a power device must be used as the output transistor.

Inverters 1 and 2 are connected to form a second astable circuit, but these are used with C – R values which produce an operating frequency of only a few Hz. The output of the low frequency astable is loosely coupled to the input of the tone generator astable by R2. This affects the timing of the tone generator astable causing increased frequency when inverter 2 output is low, and decreased frequency when it is high. In this way the tone generator is switched between two frequencies at a rate of a few Hz and a very effective alarm sound is produced.

The average current consumption of the circuit depends upon the speaker impedance and supply voltage used, and varies from approximately 300 mA when using a 15-ohm speaker and 9-volt supply to about 750 mA when using an 8-ohm speaker and 12-volt supply. Small batteries would be totally inadequate to supply this and either heavy duty batteries or a main power supply of adequate ratings must be employed as the power source.

A BD121 device is specified for Tr2 simply because this was the device used in the prototype unit. The circuit should work equally well using any power transistor capable of handling a collector current of at least two amps and having a current gain of at least twenty (2N3055, TIP41, etc.).

Auto Fade Out

Sound generators for use in burglar alarms and similar systems often incorporate circuitry which causes them to switch off some while after they have been activated. This is a sensible facility since after sounding for a few minutes the alarm will

have fulfilled its task. If it then continues to sound until the owner returns to switch it off, it is quite likely to cause considerable annoyance to neighbours.

The circuit of Fig. 8 can readily be modified so that it automatically fades out after it has been operating for some predetermined time, and the necessary modification is shown in Fig. 9. Inverter 4 is now used as a NOR gate, and so the modified circuit must employ a 4001 I.C.

As was demonstrated earlier by the exit delay burglar alarm circuit (Fig. 6), if one input of a NOR gate (or both inputs) is (are) at logic 1, then the output must go to logic 0. In the circuit of Fig. 9 the lower input of inverter 4 will be held at logic 0 by uncharged capacitor C4 when the power is initially connected to the circuit. Thus the logic state assumed by the output of this gate is determined by the upper input. In effect, with the upper input connected into circuit exactly as before, gate 4 still acts as an inverter and the circuit functions normally.

C4 will gradually charge up through R5, and after about 4 minutes the voltage fed to the lower input will reach the transition level of the gate. As this input gradually goes from logic level 0 to logic level 1, the maximum voltage achieved by the output of inverter 4 on positive going excursions will gradually reduce, causing the volume of the output signal to progressively fade. After a short time the lower input of inverter 4 will be fully at logic level 1, the output will go to logic 0, Trs1 and 2 will be cut off, and the alarm will cease to function.

L.E.D. indicator D1 is fed from the supply lines by way of current limiting resistor R6. This is to provide the user with an indication of whether or not the alarm has been triggered in his or her absence.

If required, the length of the switch off delay can be changed by altering the value of C4. Increasing its value proportionately increases the length of the delay, and reducing its value has

the opposite effect, of course. C4 must be a good quality low leakage component if the circuit is to function properly.

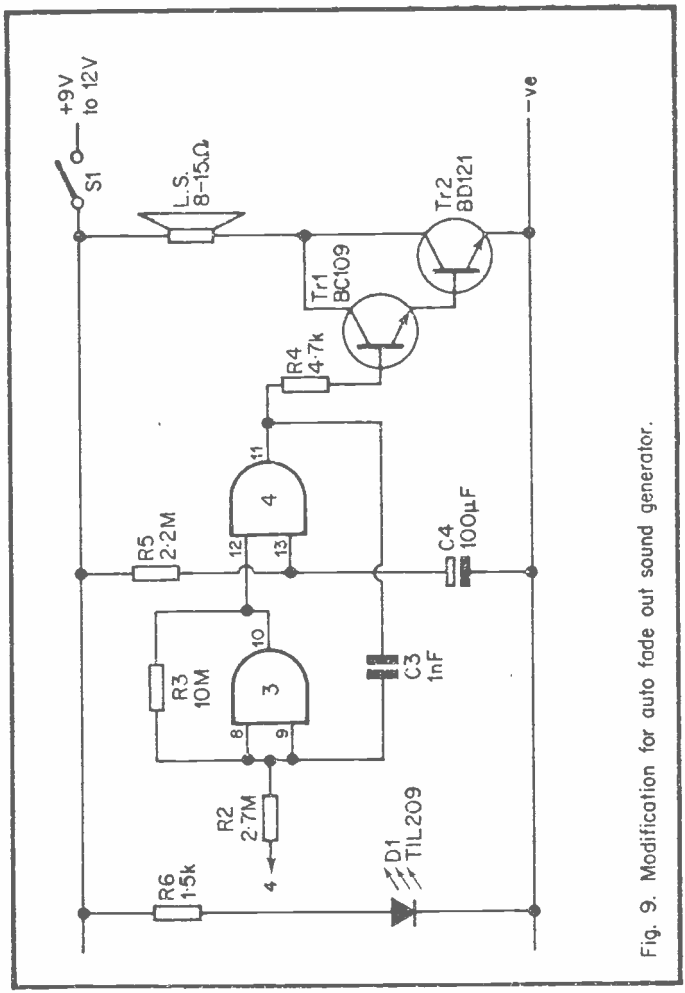


Fig. 9. Modification for auto fade out sound generator.

Doorbuzzer

To produce a really good doorbuzzer circuit is more difficult than one might expect. As mentioned earlier, a simple tone generator is easily masked by other sounds and is rather ineffective. It is also rather monotonous and unpleasant to listen to, which is obviously undesirable for a doorbell. Many types of modulated tone generator produce an effective, penetrating sound, but are also unpleasant to listen to and far from ideal as doorbuzzers.

The doorbuzzer circuit of Fig. 10 produces a very noticeable and pleasant sound. It is basically similar to the circuit of Fig. 9, but several modifications have been made.

Firstly, a doorbell does not need to have anything like the output power of a burglar alarm sound generator. In fact, it would soon become rather overbearing if it did. Therefore, a single transistor output stage providing a few hundred mW to a high impedance speaker is used. This produces a perfectly adequate sound level, and gives the unit a current consumption of something in the region of 50 to 100 mA, depending upon the impedance of the speaker used in the unit. This enables the unit to be powered from an ordinary 9-volt transistor radio type battery (PP6, PP7, etc.) if desired.

An astable multivibrator has an output waveform which is virtually a squarewave and is rich in harmonics. This produces a rather harsh tone which can be improved by filtering out some of the higher frequency harmonics. This is accomplished by C4 which forms a low pass filter in conjunction with current limiting resistor R4.

Finally, the speed of the modulator astable has been increased somewhat. It oscillates just too fast for the switching from one note to the other to be clearly heard, and this produces quite a pleasant warble type output.

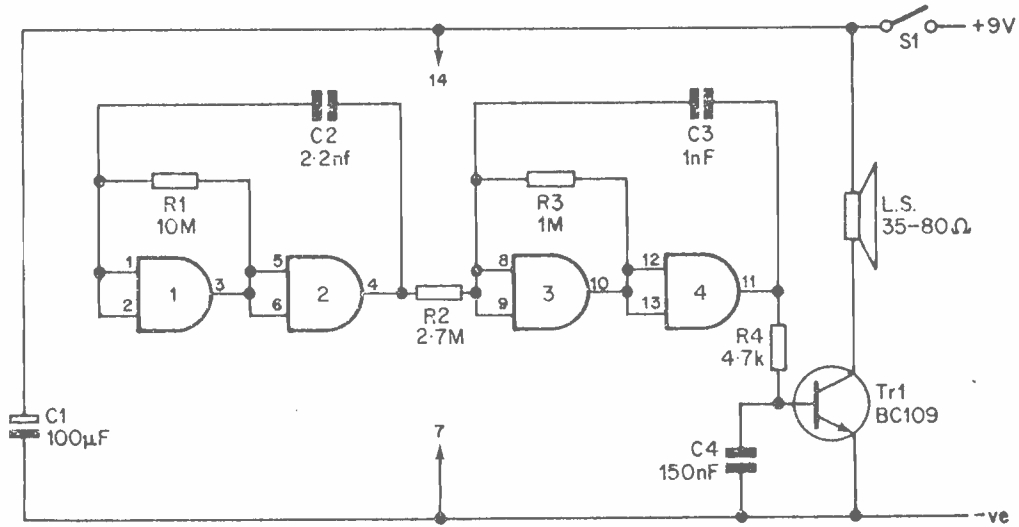


Fig. 10. Warble tone generator suitable for use as a door buzzer.

Probeless Continuity Tester

Probably most readers will be familiar with the usual type of audible continuity tester where the device emits a tone if a fairly low impedance is present across a pair of test prods. There is a less common type of continuity tester that is designed to produce an audio output if a resistance of a few Meg. ohms or less is present across two electrodes.

A unit of this type is unsuitable for some applications as stray circuit resistances would activate the circuit and indicate continuity when this was not in fact the case. There are certain applications where this does not apply, and such a unit can be quicker and easier to use.

Continuity testers of this type are often termed 'probeless', and physically they are constructed so that no probes are required. The usual form these take is a metal casing which acts as one electrode and a large screw mounted at some convenient point of the case to act as the other electrode. The two electrodes must, of course, be extremely well insulated from one another.

If a suspected blown fuse is to be tested, for example, then the metal case of the continuity tester is taken in one hand and one contact of the fuse is taken in the other hand. Touching the free contact of the fuse onto the small electrode of the tester will complete a circuit across the two electrodes through the body of the user and through the fuse, assuming that the latter is in fact functional. Due to the body resistance of the user there will obviously be quite a high resistance across the two electrodes of the tester, and it is for this reason that the unit needs to be responsive to far higher resistance than a conventional continuity tester.

The circuit diagram of the probeless continuity tester appears in Fig. 11. This is based on two NOR gates and therefore only a 4001 device should be used in this circuit.

As the circuit stands, R1 will take one input of each gate to

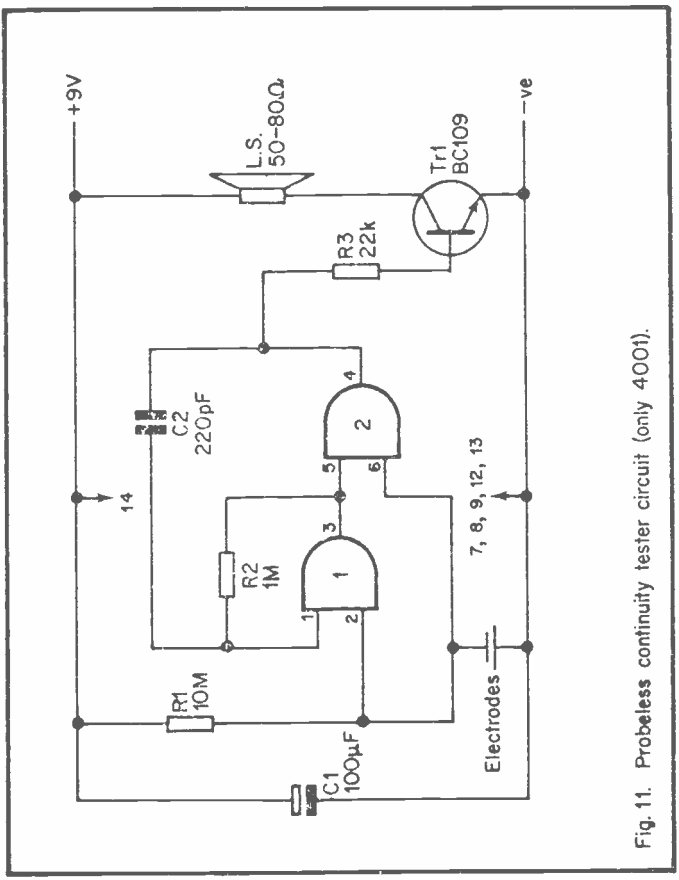


Fig. 11. Probeless continuity tester circuit (only 4001).

logic 1, and so the output of each gate will be at logic 0. Tr1 will be cut off and so only minute leakage currents will flow in the circuit. Because of this it is unnecessary for an on/off switch to be fitted to the unit.

If there is continuity across the two electrodes, or even a resistance of several Meg. ohms, the lower input of each gate will be taken below the transition voltage and they will effectively be at logic 0. The logic levels at the gate outputs are

now controlled by the upper inputs, and these are connected in a straightforward astable multivibrator circuit. The unit will therefore oscillate, and with the specified values for R2 and C2 the circuit operates at about 1 kHz or so. The output of the astable is used to drive a loudspeaker via common emitter amplifier Tr1, and so an audio tone will be produced from the speaker.

When using a continuity tester of this type it must be borne in mind that it is not suitable for all types of testing. For example, it can be used to test silicon diodes as these have reverse resistances of hundreds of Meg. ohms. The leakage current through the device will therefore be inadequate to spuriously operate the tester. The same is not true for a germanium diode though. These usually have a reverse resistance of only a few hundred k ohms and it rarely exceeds much more than a Meg. ohm. This is likely to be less than the body resistance of the user, and will certainly be low enough to activate the circuit.

Continuity Tester

The circuit of Fig. 11 can readily be modified to operate as a conventional continuity tester, and the suitably modified circuit is shown in Fig. 12. This operates in basically the same way as the original circuit.

R1 is adjusted so that the upper inputs of the two gates are just below the transistion voltage when the two test prods are shorted together. This effectively takes them to logic 0 and enables the circuit to oscillate and produce an audio tone from the loudspeaker.

If there is a resistance of more than a few hundred ohms across the test prods, this will be added to the resistance of R1 as far as the potential divider action across R1 and R2 is concerned, and the voltage applied to the upper inputs of the gates will be above the transition voltage. These inputs will, in effect, be at logic level 1, and the astable circuit action will be blocked.

Thus the circuit will not be activated by resistances of more than about two or three hundred ohms. Lower but nevertheless significant resistances will activate the circuit, but it will be apparent if there is a significant resistance across the test prods as the output level will be reduced and the tone of the output signal will change noticeably.

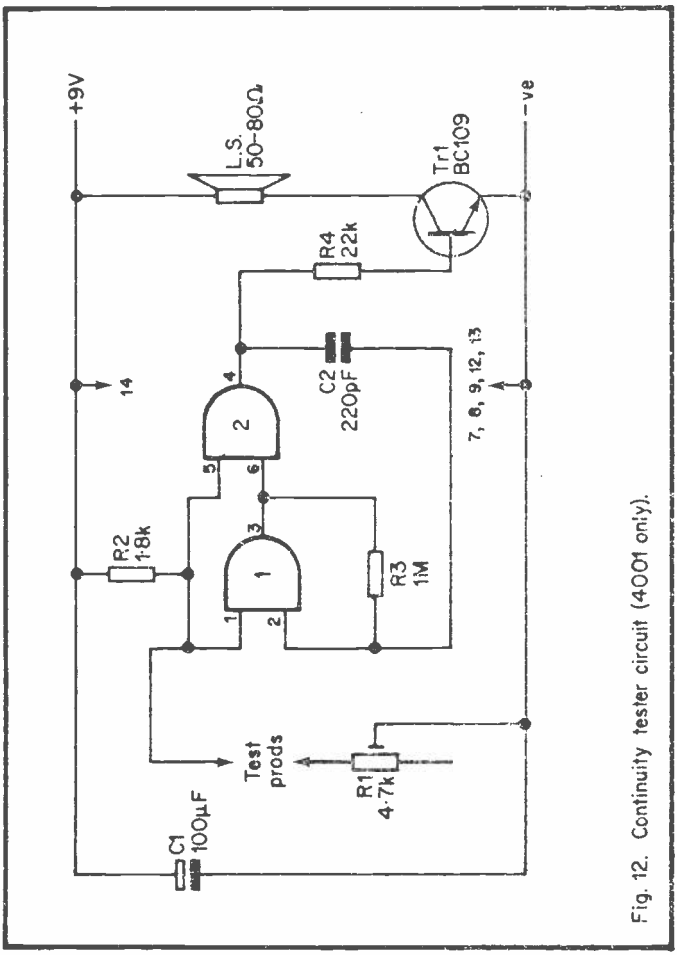


Fig. 12. Continuity tester circuit (4001 only).

Oscilloscope Calibrator

Some oscilloscopes have an internal calibrator, but it is not a feature of all instruments, and many home constructed units are without this facility.

A calibrator for an oscilloscope really just consists of a square-wave generator with an output of known peak to peak amplitude. Practical calibrators often have several outputs of known amplitude. It is normal for an oscilloscope calibrator to operate at a middle audio frequency where the gain of the instrument will not be affected by any high or low frequency roll off.

The circuit diagram of the oscilloscope calibrator is given in Fig. 13. The 9-volt battery supply is applied to a simple emitter follower regulator circuit via on/off switch S1. The regulator circuit consists of a simple Zener shunt regulator (R6 and D1) feeding an emitter follower transistor (Tr1) via preset potentiometer R5. The emitter voltage of Tr1 will be equal to its base voltage minus about 0.65 volts dropped across its base emitter voltage. R5 is adjusted to produce a stabilised potential of about 5.65 volts at Tr1 base, and this gives an emitter voltage of 5 volts. Tr1 operates as a current amplifier, and although its base is fed from a fairly high impedance source, the output at its emitter is at a comparatively low impedance which is suitable to drive the main calibrator circuitry.

Inverters 1 and 2 are connected in the astable mode and R1 plus C3 produce an operating frequency of approximately 1 kHz. The output from the astable is fed to a buffer amplifier which consists of inverters 3 and 4 wired in parallel. This gives half the output impedance of buffer stage using a single inverter as the parallel operation gives two output transistors to source or sink the load currents.

The complementary output stages of CMOS devices produce high and low output states that are virtually equal to the positive and negative supply rails when the outputs are unload-

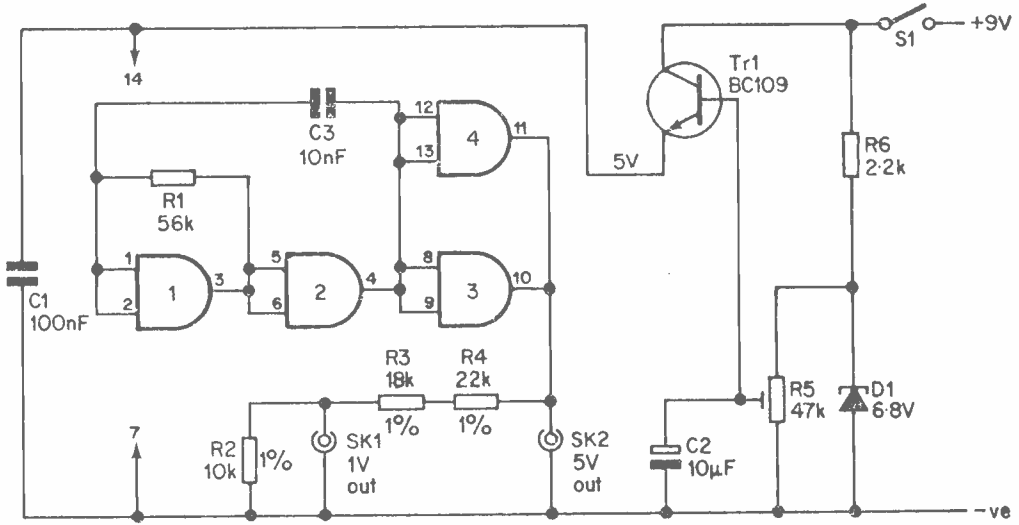


Fig. 13. 1V and 5V peak to peak oscilloscope calibrator (approx. 1KHz).

ed or only lightly loaded. This means that by accurately setting the supply voltage to the calibrator at 5 volts, a peak to peak amplitude of 5 volts peak to peak will be produced at the buffer stage output. This enables the peak to peak output voltage to be adjusted to the correct level using just a multimeter, and a calibrated oscilloscope is not required in order to set the finished unit up correctly.

R2 and R4 form a simple attenuator and produces an output signal of 1 volt peak to peak at SK1. Of course, a more complicated attenuator providing further output levels can be used if necessary. In order to obtain good accuracy it is essential that the attenuator should only lightly load the output of the astable. It is also essential that the scope should only lightly load the circuit, but as most instruments have an input impedance of something in the region of 1 Meg. ohm, there should be no problems here.

The only adjustment required to the finished unit is the setting up of R5, and as was pointed out earlier, this is merely adjusted to produce precisely 5 volts at Tr1 emitter.

Logic Probe

A logic probe can be extremely useful when troubleshooting on logic circuits, whether they are simple designs of the type provided in this book or more complicated units such as digital frequency meters, etc. The purpose of a logic probe is to indicate whether the point to which the probe tip is connected is at logic 0, logic 1, or some indefinite level. The latter can either be some fixed state between the two logic levels or rapidly switching between the two states.

A simple logic probe circuit is shown in Fig. 14 and this uses two L.E.D. indicators to show the state of the test point. The circuit requires a supply current of no more than a few mA, and so it can be powered from the circuit under test. This is common practice with logic probe designs.

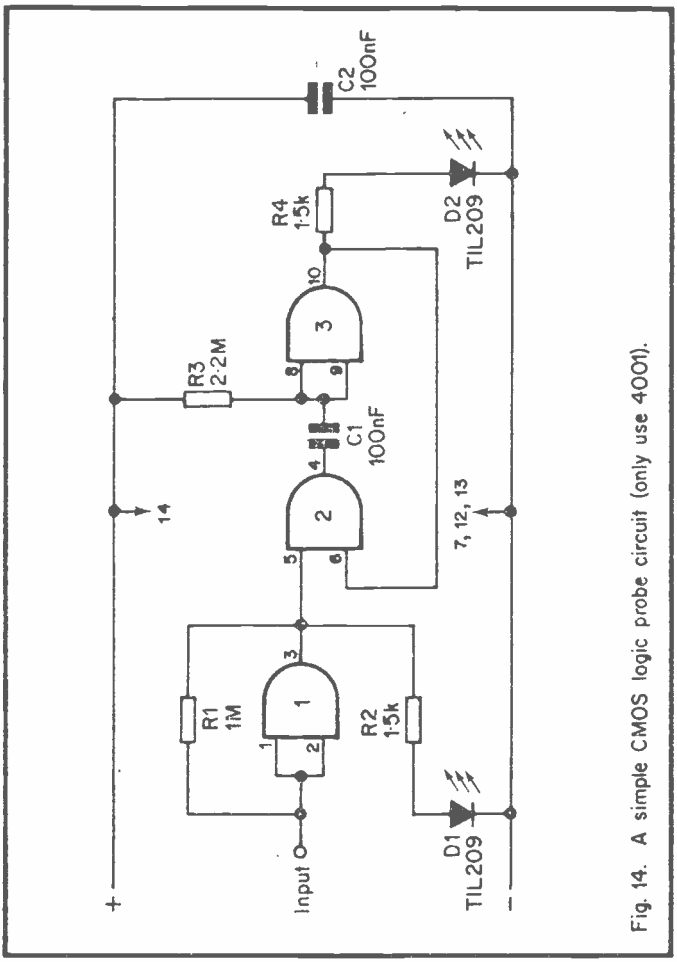


Fig. 14. A simple CMOS logic probe circuit (only use 4001).

Inverter 1 is biased to operate as an amplifier, and its output feeds one of the L.E.D. indicators (D1) via current limiting resistor R2. Under quiescent conditions the output of inverter 1 will be at approximately half the supply potential, and so D1 will light up, but not at full brightness.

The input signal is applied to inverter 1 input, and a logic 1 input state will cause the output of inverter 1 to go low. This will be indicated by the L.E.D. indicator switching off. A logic 0 input will cause inverter 1 output to go high, and this will be indicated by the L.E.D. indicator coming on at full brightness. An indefinite input level, whether pulsing or between the two logic levels, will cause the L.E.D. indicator to come on, but at less than full brightness.

Some additional circuitry and a second indicator lamp are used to enable the circuit to distinguish between a floating indefinite input state and a pulsing input. Inverters 2 and 3 are connected to form a simple non-retriggerable monostable multivibrator.

This type of circuit produces an output pulse of fixed duration when it is triggered by an input pulse. The length of the output pulse is determined by an R – C timing circuit, and this function is performed by R3 plus C1 in this case. These produce an output pulse of very approximately 150 mS in length.

Thus, if there is a pulsing input the monostable will be triggered and its output will go high for about 150 mS. It will then return to the low state but another input pulse will almost immediately trigger the circuit once again, and the output will go high for a further period of 150 mS. The circuit will be continuously triggered and the output will be in the high state for virtually 100% of the time.

L.E.D. indicator D2 is driven from the output of the monostable via current limiting resistor R4, and D2 will therefore come on at (for all practical purposes) full brilliance in the presence of a fast pulsing input. With the input at a static input level the monostable will not be triggered and D2 will not come on. In this way the necessary discrimination between a pulsing input and a static indefinite input state is obtained. Of course, with a slowly pulsing input, D2 and its associated circuitry are not necessary as D1 will flash on and off at a slow enough rate for this action to be clearly seen.

It should be noted that gate 2 of this circuit is used as a NOR gate and not as an inverter, and only a 4001 device should be employed in this design.

Chapter 3

AMPLIFIER, TRIGGER AND GATE PROJECTS

As we have already seen in some of the projects described in the previous chapter, a CMOS inverter can be biased to act as a linear amplifier merely by connecting a resistor between the input and output, as shown in Fig. 15 (a). When the supply is first connected to the circuit the input will be at logic 0, and so the output voltage will start to rise to logic 1. However, due to the coupling between input and output of the inverter through the bias resistor, as the output voltage reaches the transition voltage of the inverter the input will begin to go from logic 0 to logic 1. This prevents the output from rising further in voltage due to a straightforward negative feedback action. Therefore, under quiescent conditions the output and input are both at roughly half the supply voltage.

In this state both the p channel and n channel transistors of the inverter are switched on to some degree, and so an appreciable current (a few mA) will be consumed by the circuit. A positive input voltage will increase the bias on the n channel device and reduce the bias on the p channel transistor. This decreases the impedance of n channel transistor and increases the impedance of the p channel device. This causes a negative going swing in the output voltage by a simple potential divider action. A negative input signal unbalances the biasing of the two transistors in the opposite direction and produces a positive change in the output voltage.

The voltage gain of this type of CMOS amplifier is approximately 50 times. The value of the bias resistor is not critical and it is this value that controls the input impedance of the amplifier. The input impedance is roughly equal to the bias resistor value divided by 50.

CMOS amplifiers provide a reasonably good performance from d.c. to frequencies of a few MHz. However, at audio frequen-

cies the noise performance of MOS devices is not as good as Jugfets or low noise silicon transistors, and it is recommended that CMOS amplifiers should not be used in Hi-Fi or other critical applications.

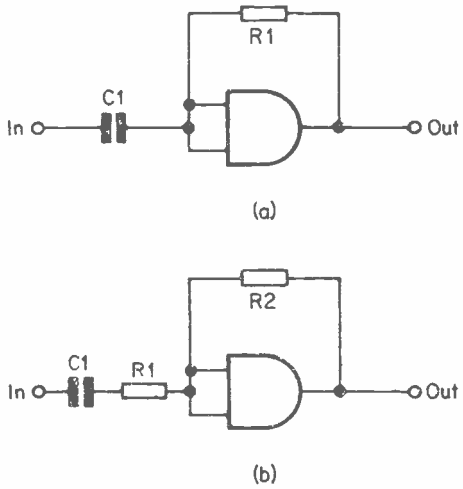


Fig. 15. (a) Basic method of using a CMOS inverter as a simple amplifier. (b) Alternative CMOS amplifier configuration.

Alternative Amplifier

A slightly different form of CMOS amplifier is shown in the circuit of Fig. 15(b). This uses operational amplifier techniques to determine the voltage gain and input impedance. R1 is given a value which is equal to the required input impedance, and this is then multiplied by the required voltage gain in order to find the correct value for R2. The maximum voltage gain that can be attained is about 50 times (i.e. the open loop gain of the CMOS amplifier).

Since R1 forms a low pass filter in conjunction with the input capacitance of the inverter, this type of amplifier will not work well at high frequencies, and if R1 has a very high value it will fail to work at all at frequencies above the audio range. It will work well at d.c. and audio frequencies, and is useful where a low gain high input impedance buffer amplifier is needed.

High Impedance Voltmeter

An ordinary multimeter usually has a sensitivity of 20 k/volt on the d.c. voltage measuring ranges. This simply means that for one volt of full scale deflection sensitivity there is 20 k of resistance between the two test prods. Thus, for example, on the 5-volt range a normal multimeter will have a resistance of 100 k.

Although such a multimeter obviously has a reasonably high resistance even on the lower voltage ranges, this resistance can, under certain circumstances, be low enough to have a significant effect on the test circuit. It is high impedance circuits that can cause problems with the multimeter loading the circuit to such a degree that the test voltage is greatly reduced when the multimeter is connected into circuit. This is most likely to occur when making very low voltage readings as it is on the lower voltage ranges that the resistance of the multimeter is at its lowest. However, this problem can also manifest itself when taking comparatively high voltage readings.

The normal way of overcoming this problem is to use a high impedance voltmeter when making voltage tests on high impedance circuits. This type of voltmeter uses an amplifier ahead of the meter in order to reduce the input current needed to produce full scale deflection of the meter.

The circuit diagram of a very simple but accurate high impedance voltmeter using a CMOS amplifier is shown in Fig. 16. The inverter is biased by R5 and so about half the supply voltage appears at the output of the inverter. R6, R7, and M1

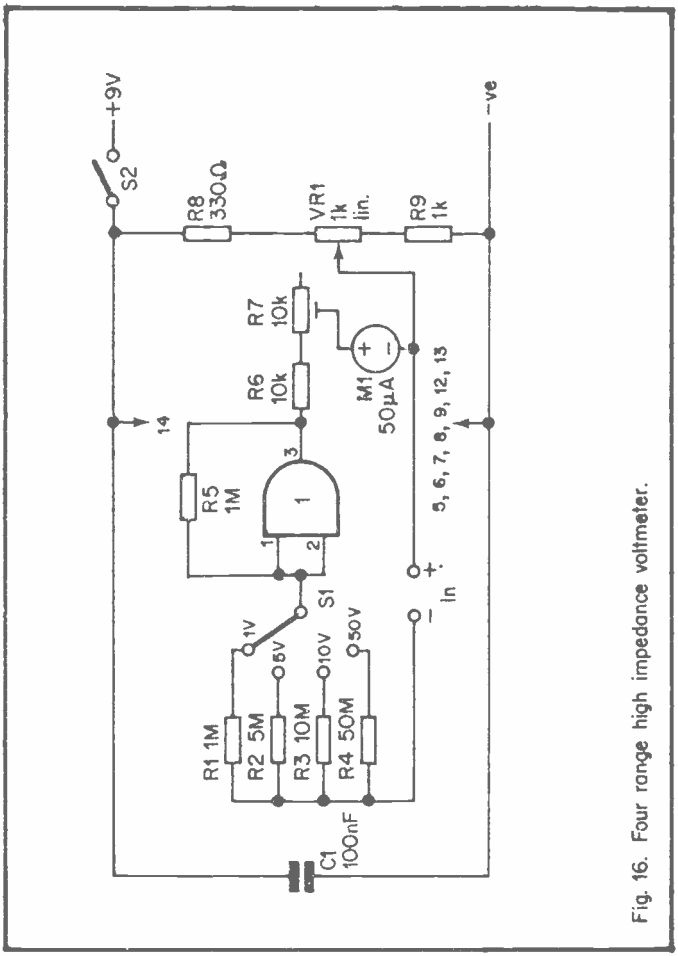


Fig. 16. Four range high impedance voltmeter.

form a straightforward voltmeter circuit having a sensitivity of 1 volt f.s.d., R6 being adjusted to set the sensitivity at this level. VR1 is adjusted to produce a voltage at the negative terminal of VR1 that is precisely the same as that present at the output of the inverter, and so under quiescent conditions there is no voltage developed across the meter, and it is zeroed.

In the absence of an input voltage there is no voltage present across the test prods as R5 balances the input and output voltages of the inverter. With S1 in the position shown (1 volt range), if we assume a 1-volt input signal of the correct polarity is applied to the circuit, this will take the input of the inverter negative and will cause its output to go positive. It will, in fact, go 1 volt positive and produce f.s.d. of M1. With the output 1 volt positive the current through R5 precisely cancels that through R1 and maintains the balance of the circuit. If the input voltage is only (say) 0.5 volts, then the output will only need to go 0.5 volts positive in order to balance the circuit.

The circuit therefore provides unity gain, but it provides a current gain of 50 times as the input signal is loaded by the 1 Meg. ohm resistance of R1 and the output feeds the 20 k resistance of the meter circuitry. Thus only 1 microamp needs to flow in the input circuit in order to produce f.s.d. on the 50-microamp meter used in the M1 position. This gives the unit an input sensitivity of 1 Meg. ohm per volt which is more than adequate for any normal amateur requirements.

Four voltage measuring ranges are provided by having four different input resistors (R1 to R4), the appropriate resistor being selected by S1. By increasing the value of the series input resistor, the input voltage needed in order to produce a given level of unbalance of the amplifier is increased proportionately. For example, on the 5-volt range an input voltage of 1 volt will produce a current flow of 0.2 microamps through R2. The output of the inverter only needs to go 0.2 volts positive in order to produce a countering 0.2 microamp current flow to redress the balance of the amplifier. Therefore, 5 volts is needed in order to produce f.s.d. of M1.

It should perhaps be pointed out that the above explanation of the circuit action is slightly idealised in that it assumes the amplifier to have an open loop gain that is infinite, whereas this gain is only actually about 50 times. This merely means that the closed loop gain of the circuit is a little less than the

theoretical value, and in practice R7 has to be adjusted for a f.s.d. sensitivity of a little less than 1 volt in order to compensate for this.

Adjustment

Start with R7 adjusted for maximum resistance and VR1 set for almost minimum voltage at its slider. When power is applied to the circuit the meter should give a strong positive indication and VR1 is immediately adjusted to zero the meter. R7 is then adjusted to give the circuit the correct sensitivity. One way of achieving this is to measure the precise voltage of a 9-volt battery using a multimeter. Then with the high impedance voltmeter switched to the 10-volt range, connect the battery to the input and adjust R7 to produce the correct reading on M1.

As the supply voltage falls with battery ageing it may occasionally be necessary to slightly readjust VR1 to re-zero the meter. If a stabilised supply is used this will not be necessary and VR1 can be replaced by a preset component.

Ideally resistors R1 to R5 should all have a tolerance of 2% or better, but in the cases of R2, R3 and R4 it is unlikely that suitable components will be available. This necessitates the use of either lower tolerance components or several close tolerance resistors wired in series to make up the required value. R4 has an exceptionally high value, and this can be made up from five 10 Meg. resistors connected in series (5% tolerance components should give good results in practice here).

Sound Activated Switch

Sound activated switches have numerous uses, and can be used in such applications as baby alarms, telephone repeaters, voice operated tape recorders (for dictation), VOX systems in radio communication equipment, and even in burglar systems.

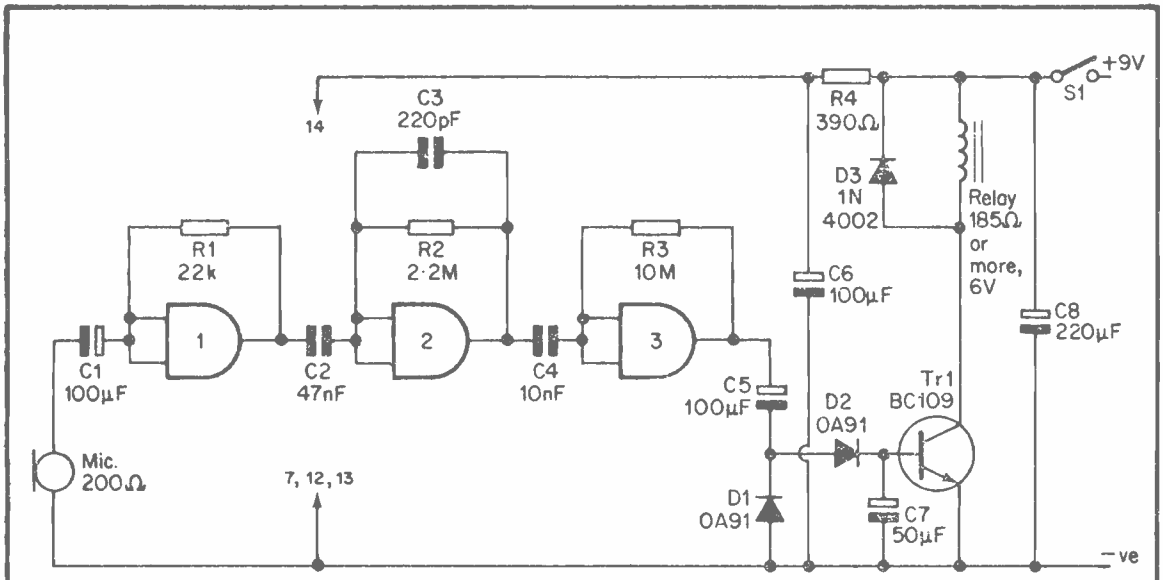


Fig. 17. A sound activated switch based on CMOS amplifiers.

Fig. 17 shows the circuit diagram of a simple sound activated switch of adequate sensitivity for most purposes. The microphone is a low impedance dynamic type of the kind used with cassette recorders, although any other low impedance microphone should work equally well. The output from the microphone is fed to a three stage CMOS amplifier which provides a high overall voltage gain. C3 rolls of the high frequency response of the circuit slightly and this is necessary in order to aid stability.

The output of the amplifier is fed to a simple rectifier and smoothing network using D1, D2 and C7. In the presence of a reasonably strong microphone signal the positive bias voltage produced across C7 will be sufficient to switch on Tr1 and activate the relay. A pair of relay contacts are used to control the ancillary equipment.

The circuit incorporates what is termed hysteresis. This simply means that when the microphone picks up a sound the relay will very quickly be energised, but once activated the relay will hold in the on state for about 1 second even if the sound ceases. The length of the switch off delay can be increased or decreased to some extent by raising or lowering the value of C7. Hysteresis is a desirable feature in virtually all applications of the circuit as it enables the unit to quickly respond to an input signal, but prevents rapid switching on and off of the relay by a signal of intermittent strength (which includes just about any likely sound source including ordinary speech).

Due to the high gain of the circuit it is essential that earth feedback loops are avoided as instability will otherwise almost certainly result. For this reason it is recommended that this circuit should not be undertaken by inexperienced constructors.

Speech at normal volumes will operate the circuit at a distance of about 2 metres, but the exact sensitivity of the unit is largely dependent upon the efficiency of the particular microphone used. Microphones having comparatively large inserts seem to

give greater output than smaller types in the author's experience.

Voltage Controlled Amplifier

Enhancement MOSFETs, which are the devices which form the basis of CMOS I.C.s, make excellent voltage controlled resistors for use in voltage controlled attenuators, voltage controlled filters, etc. In theory it is possible to connect CMOS inverters and certain other devices in such a way that one transistor is isolated for use in this type of application, but in practice this is often not successful with modern CMOS devices. This is presumably due to the protection circuits at the inputs of the devices blocking the operation of such circuits.

A two input NOR gate can be used as a simple voltage controlled amplifier when connected in the manner shown in Fig. 18, and input protection circuits do not seem to have an adverse effect on this unit (not with the various 4001s tried by the author anyway). The circuit does have a drawback in that as the gain of the amplifier is varied, the static output voltage of the circuit changes. This precludes its use in applications where rapid changes in gain will occur, as this would generate a strong a.c. signal at the output. It seems to work perfectly well in simple applications though, and it can be used as a d.c. remote volume control. This type of circuit is used in remote volume controls for radios, T.V.s, etc., and has the advantage over ordinary volume controls that only d.c. levels are handled by the connecting lead. This enables a decoupling capacitor (C2) to be used to filter out any stray hum or noise that is picked up in the cable. Even if a long, unscreened connecting cable is used, there should be no significant noise pick-up in the connecting cable.

R1 and R2 are simply adjusted so that VR1 can adjust the gain of the amplifier from zero to maximum, but there should not be a range of settings at either end of VR1's travel where there is no effect on the gain of the circuit. This is probably most

easily accomplished by starting with R1 and R2 at minimum resistance, and then gradually increasing their resistances by trial and error until the full adjustment range of VR1 is needed in order to vary the gain from maximum to minimum.

Some voltage controlled amplifier circuits have only a limited control range, but this is not the case with this circuit. The maximum voltage gain of 50 times can be reduced to what, for all practical purposes, can be regarded as an infinite attenuation. The circuit gain reduces with increasing voltage at VR1 slider, and as the gain reduces so does the quiescent output voltage. This means that the maximum output voltage swing

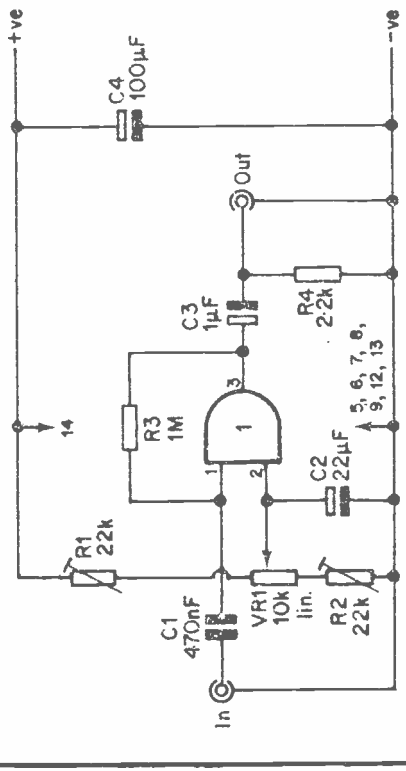


Fig. 18. A CMOS voltage controlled amplifier using a NOR gate.

that the unit can handle reduces as the gain is turned back, but this is of no practical consequence as the output signal amplitude obviously reduces when the gain is turned back.

Voltage Controlled Attenuator

In many applications the voltage gain of 50 times provided by the previous circuit will not be needed, and a circuit having a

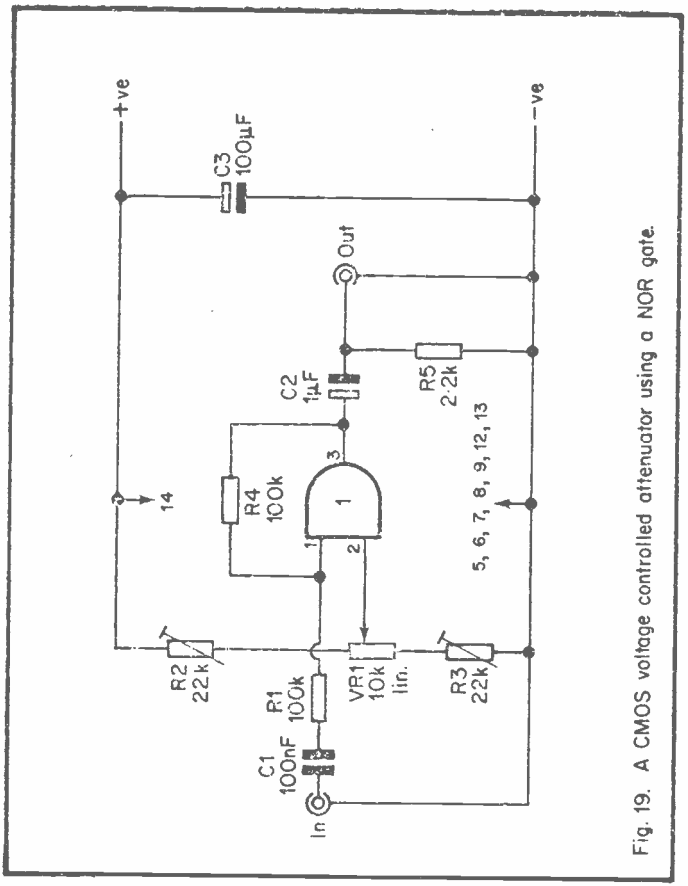


Fig. 19. A CMOS voltage controlled attenuator using a NOR gate.

maximum gain of unity, like an ordinary volume control, will be all that is required. In other words, a voltage controlled attenuator rather than an amplifier. The circuit of Fig. 18 can be readily modified to function in this manner by using a negative feedback loop to limit the maximum gain of the circuit to unity. The modified circuit appears in Fig. 19. R1 and R4 set the maximum gain at one, and the gain can be increased somewhat if necessary by increasing R4 in value (maximum voltage gain is approximately equal to R4 divided by R1).

Automatic Fader

It is possible to use a CMOS voltage controlled amplifier or attenuator in simple automatic audio control circuits, and an example of this is shown in Fig. 20. This gives the circuit diagram of a simple automatic fader using CMOS gates. An auto fader is a unit which will attenuate a secondary channel in the presence of a signal on the main channel. It can, for instance, be used during slide or film shows to automatically fade background music during the commentary. Circuits of this type are often incorporated in disco equipment.

Gate 1 is used as the voltage controlled attenuator, and R3 is adjusted to produce a control voltage that is just low enough to produce maximum gain through the attenuator circuit. Gate 3 is used as an active mixer circuit and it is used to mix the control input signal and the output from the attenuator.

Part of the control signal is fed to the input of an amplifier which is based on gate 2. The amplified output from this is fed via C5 and R7 to a simple rectifier and smoothing network using D1, D2 and C3. In the presence of a strong input signal at the control input a large positive bias will be developed across C3 and will increase the control voltage of the V.C.A. circuit. This causes a reduction in the gain of the V.C.A. and fades out the controlled signal in the required manner.

The gain between the controlled input and the output is about

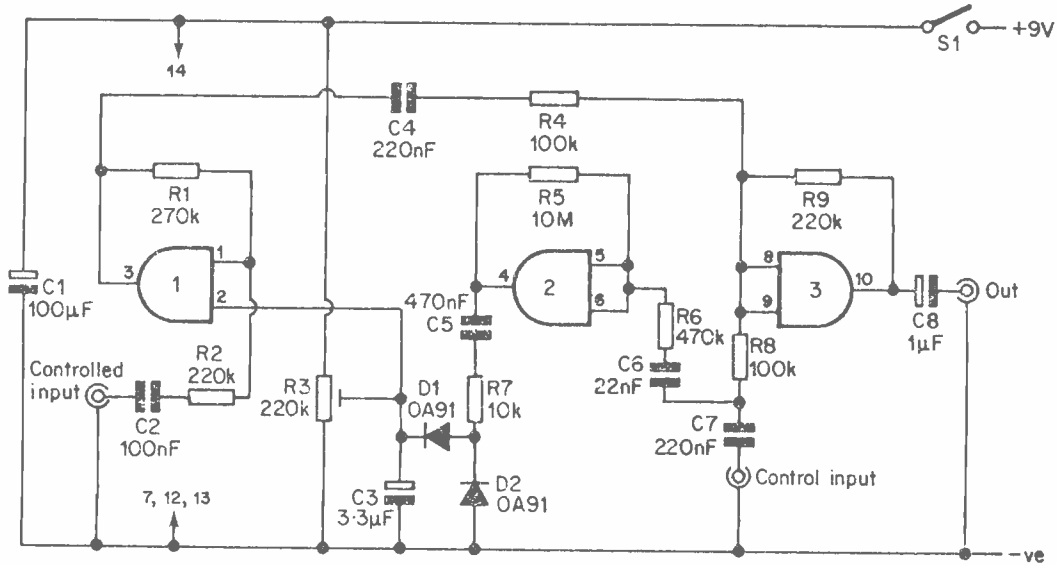


Fig. 20. The circuit of a simple CMOS automatic fader (4001 only).

6 dB (two times) with no significant input at the control input. There is a similar level of gain between the control input and the output. A signal level of a few hundred mV r.m.s. at the control input will fade out controlled input by 20 dB (ten times) or more. The amount of fade produced by a given input level at the control input can be varied to some extent by altering the value of R6. Increasing its value reduces the amount of fade, and reducing its value increases the level of fade.

The circuit has hysteresis so that the controlled input is quickly (but considerably less than instantaneously) faded out when an input signal is applied to the control input, but the controlled signal is smoothly returned to full level at a comparatively slow rate when the signal ceases. This gives an agreeable sounding circuit action and prevents modulation of the controlled signal by the control signal.

Morse Practice Oscillator

CMOS amplifiers make a good basis for various types of waveform generator, and an example of such a circuit is shown in Fig. 21. This is designed as a morse practice oscillator, and produces a sinewave output (the waveform produced by a real c.w. signal).

Inverters 1 and 2 are both biased as amplifiers and are connected in series. The input and output of the amplifier as a whole are therefore in phase, and sufficient feedback between the two will cause the circuit to oscillate. Feedback is applied over the circuit by the Wien network which consists of C1, R1, R2 and C3. This is a frequency selective network which has a peak response at approximately 1 kHz, and so the circuit oscillates at this frequency.

The CMOS amplifiers have quite a high combined voltage gain, but a voltage gain of only about three times is needed in order to maintain oscillation. This causes the circuit to oscillate very violently causing the output signal to be severely clipped un-

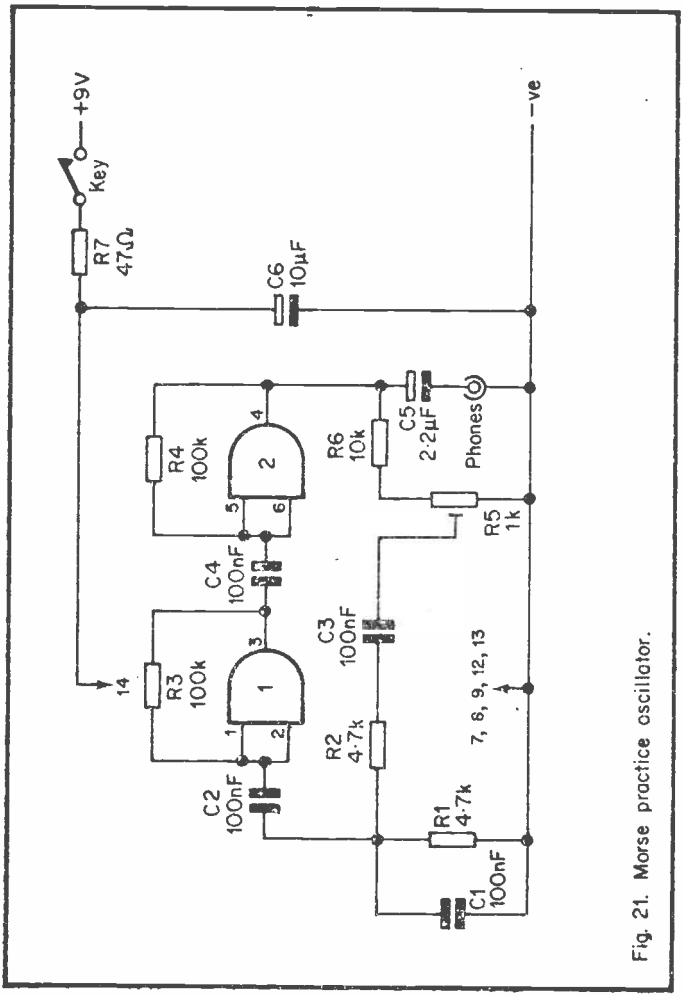


Fig. 21. Morse practice oscillator.

less steps are taken to reduce the feedback gain. The necessary reduction in the feedback gain is provided by R5 and R6 which form a simple variable attenuator at the output of the amplifier. The output to the Wien network is taken from the slider of R5 and the latter is adjusted so that the circuit is just gently oscillating, and a sinewave output of reasonable amplitude and purity is obtained.

C6 is a supply decoupling capacitor, and its value is chosen to produce a pleasant keying characteristic. R7 also helps to give a good keying characteristic, and acts as a current limiting resistor when the key contacts close and C6 begins to charge up. This reduces the risk of sparking at the key contacts, which would give a comparatively short contact life.

The output will feed any type of high impedance headphones or earpiece. It should also work well with medium impedance types, but only poor results are likely to be obtained using low impedance phones or a low impedance earpiece. For loudspeaker operation the output of the unit can be fed to virtually any amplifier/speaker unit as the output signal level is more than adequate to drive any normal amplifier.

The setting of R5 is not very critical, but it should not be adjusted for barely sufficient feedback to support oscillation. This will give a very pure output, but the volume will be rather low and may well provide unreliable operation. Excessive feedback will probably produce perfectly acceptable results, but the output note will be slightly clipped and thus comparatively rough and unpleasant to listen to for long periods.

Light Change Detector

Several light operated switch projects are covered in the '50 CMOS I.C. Projects' book, but these are of the usual type where the circuit is triggered when the photocell reaches a certain level of illumination. This circuit is rather different in that it is not triggered by any particular light level, but by fairly rapid changes in light level. This type of circuit is not suitable for as wide a range of applications as the more conventional type of light operated switch. However, it can be used as a simple form of proximity detector in burglar alarms and other applications, and it makes an interesting project for the experimenter.

The circuit diagram of the unit is shown in Fig. 22. The light detector circuit consists of R1 and PCC1. PCC1 is a cadmium

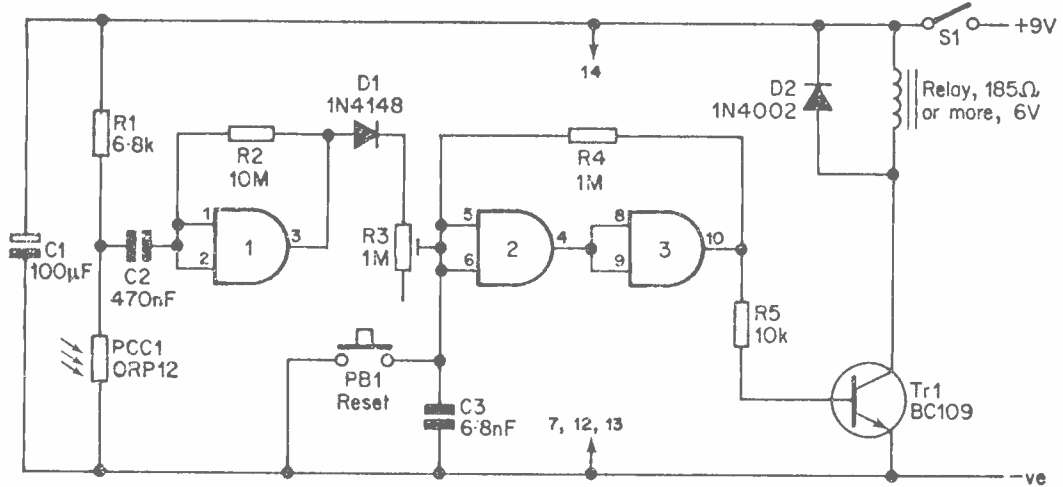


Fig. 22. High level change detector circuit.

sulphide photoresistor, and its resistance varies from more than 10 Meg. ohms in total darkness to only a few tens of ohms in bright conditions. The voltage at the junction of R1 and PCC1 therefore varies according to the light level received by PCC1.

Inverter 1 is biased as an amplifier by R2, and its input is fed from the light detector circuit via C2. The latter blocks the d.c. level produced by the photocell circuit from entering the amplifier, and neither will it couple any slow changes in this voltage (such as those caused by natural changes in the ambient light level) into the amplifier input. Any rapid changes in light level, possibly caused by someones shadow passing across the photocell for example, will be fed into the input of the amplifier by C2. This will result in a comparatively large positive and negative output voltage swing from the amplifier.

Inverters 2 and 3 are connected as a sort of Schmitt trigger circuit. When S1 is initially closed and power is applied to the circuit, C3 will tend to hold inverter 2 input at logic 0 and so inverter 2 output will go high. Inverter 3 input will be driven low and its output will go low.

Under quiescent conditions a small current will flow through D1, R3, R4 and the output circuit of inverter 3 from the output of inverter 1. R3 is adjusted for a sufficiently high resistance to ensure that the potential divider action across these components produces a voltage at inverter 2 input that is below the transition voltage of this inverter. The circuit will therefore remain with inverter 3 output in the low state, Tr1 cut off, and the relay not energised.

If the photocell is subjected to a rapid change in light level, on positive excursions at inverter 1 output the voltage at inverter 1 input will be raised above the transition voltage and inverter 3 output will start to go positive. Positive feedback through R4 causes the circuit to rapidly trigger to the state where inverter 2 input and inverter 3 output are both in the high logic state. The circuit will not be taken

back to its original state on negative going excursions at inverter 1 output as D1 will be reverse biased and will not provide the necessary coupling. The circuit will therefore latch with inverter 3 output high, Tr1 switched on, and the relay energised.

PB1 can be used to take the circuit back to its original state by briefly short circuiting inverter 1 input to the negative supply rail, and this switch acts as the reset control.

R3 is adjusted to the correct value empirically, and it should have the lowest resistance setting which does not cause the unit to be triggered when the on/off switch S1 is closed. The unit should then have quite good sensitivity and freedom from spurious triggering. Units of this type are usually quite effective at detecting someone moving around the room in which the photocell is situated as the lighting in most rooms is well diffused, and a multitude of small shadows are therefore produced. These are usually enough to trigger the unit if they pass over the photocell. The light from an intruder's torch should also be sufficient to trigger the unit, even if it is not shone directly onto the photocell. The photocell can be remotely located from the rest of the unit, incidentally, but a screened connecting cable should be used.

Under Voltage Cut-out

Some items of electronic equipment are apt to malfunction in some way if their supply voltage falls below some critical level. While in some cases such a malfunction will be quite apparent, this is not always the case, and misleading results might be obtained from the equipment without the user realising that there is anything wrong.

One way around this is to fit a circuit to the equipment that will cut off the supply if it falls below some preset level. Circuits of this type are usually fitted to electronic calculators, for example. A simple under voltage cut-out circuit is shown in Fig. 23. R1 is adjusted so that with an adequate supply

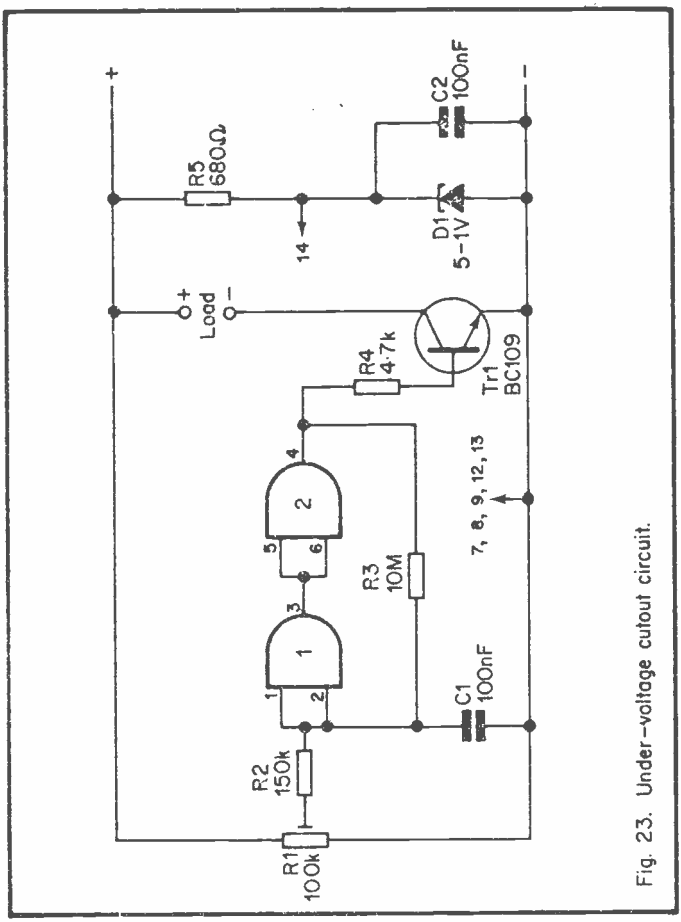


Fig. 23. Under-voltage cutout circuit.

present there is sufficient voltage at its slider to take inverter 1 input to logic state 1. This results in the output of inverter 2 being in the high state, and so Tr1 is driven hard on by the base current it receives through R4. The load therefore receives the full supply voltage, minus a few tens of millivolts dropped across the emitter–collector terminals of Tr1.

If the supply voltage begins to fall below the critical level, the

voltage at inverter 1 input will be in the transition region and the output of inverter 1 will begin to go high. As it does so it drives inverter 2 input high, and so inverter 2 output begins to go low.

Due to the coupling via R3, as inverter 2 output swings lower in voltage it causes a reduction in the voltage at the input of inverter 1. This causes inverter 2 output to swing even lower in voltage, and a regenerative action continues until inverter 2 output is fully at logic 0. When this happens, Tr1 becomes cut off and the load is no longer supplied with current.

The transition voltage of a CMOS gate varies considerably with changes in supply potential, and so a stabilised supply for the CMOS I.C. is needed in order to ensure a reliable circuit action. Such a supply is provided by the simple Zener shunt regulator which R5, C2 and D1 comprise.

The circuit has a degree of hysteresis, which simply means that if, for example, the circuit triggers to the off state at a supply potential of 9 volts, the supply voltage must rise a little way above this level in order to trigger the unit back to the on state. This is due to the fact that R3 tends to hold to input of the trigger circuit low when the output is low, or high when the output is high. This produces a slight inequality in the switch-off and switch-on voltages.

The hysteresis is a desirable feature as the supply voltage is likely to rise slightly when the cut-out operates and the supply loading is reduced. This could result in the circuit breaking into oscillation if hysteresis was absent. Indeed, it is still possible that this could happen, and it may be necessary to increase the hysteresis to prevent this from occurring. It is merely necessary to reduce the value of R3 somewhat in order to increase the level of hysteresis. C1 also aids the stability of the circuit, and decouples any stray pick-up at the input of the trigger circuit.

In order to set up R1 correctly it is necessary to connect the circuit to a supply voltage that is equal to the desired cut-out

voltage. Start with R1 adjusted for maximum slider voltage, and then slowly back it off just far enough to cause the cut-out to operate.

The circuit will operate at threshold voltages down to about 5 volts. Preferably, the supply voltage should not exceed 15 volts if the I.C. used is an 'A' series device, or 18 volts if it is a 'B' series device. A maximum load current of 100 mA can be handled by the BC109 specified for the Tr1 position, but this can be increased by using a Darlington power device in its place (or a discrete equivalent).

Over Voltage Cut-out

Automatic cut-outs can also be used in applications where it is possible that the supply voltage will rise to a level that will cause the main equipment to malfunction, or perhaps even cause damage. The circuit of Fig. 23 can be modified to operate as an over voltage cut-out simply by interposing an inverter stage between the output of the trigger circuit and the base feed resistor of Tr1. This is shown in the circuit diagram of Fig. 24.

In general, the notes on using and adjusting the under voltage cut-out also apply to this unit. However, when adjusting R1 it is initially set for minimum slider voltage, and then it is adjusted for just sufficient slider voltage to cause the cut-out to be activated.

Thermostat

Electronic thermostats can provide very high levels of performance and can be used in photography, to control room temperature, heated aquariums, and refrigeration units, and in many other applications.

Fig. 25 shows the circuit diagram of a simple CMOS thermostat which provides a high level of performance. Th1 is a

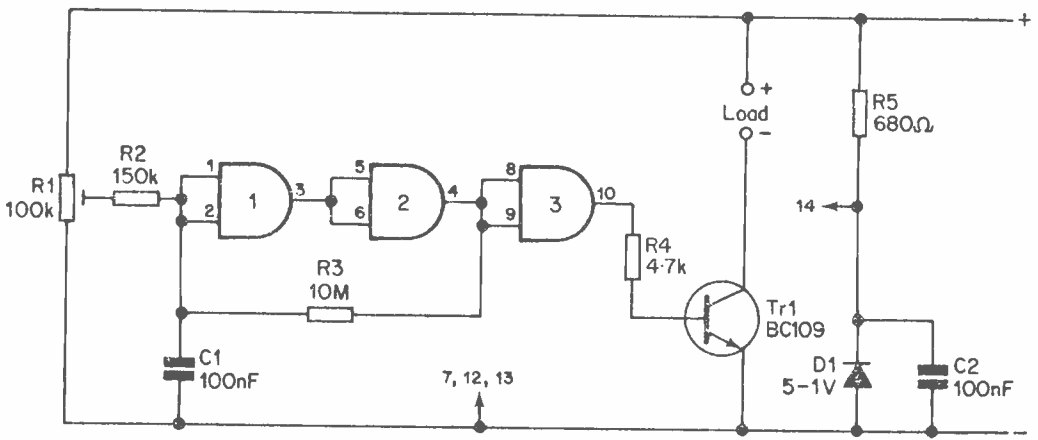


Fig. 24. Modification to circuit of Fig. 23 for over-voltage cut-out.

negative temperature coefficient thermistor and it is mounted in a probe that it situated in the environment which is to be controlled. The thermistor is connected as part of a potential divider which is wired across the supply lines, R1 forming the other section of this circuit. The resistance of Th1 varies with changes in its temperature, with increasing temperature causing a reduction in its resistance. The voltage at the junction of Th1 and R1 therefore rises and falls as the temperature of Th1 rises and falls.

Inverters 2 and 3 together with R2 and R3 form a simple Schmitt trigger circuit. The basic action of this type of circuit has been described in some of the previous sections of this book, and will not be repeated here. Suffice it to say that if the voltage at the input of the circuit goes above a certain threshold level the output of the circuit will trigger from logic 0 to logic 1. If the input voltage then falls somewhat and goes below a second and somewhat lower threshold voltage, the output triggers back from logic 1 to logic 0.

The Schmitt trigger circuit is fed from the thermistor potential divider circuit via a simple amplifier stage using inverter 1. R1 is adjusted so that when Th1 falls below the required thermostat temperature the output voltage of inverter 3 is at a just high enough voltage to switch the Schmitt trigger to the high output state. Tr1 is then switched on by the base current it receives from the Schmitt trigger via R4, and power is applied to the relay coil which forms the collector load for Tr1. A pair of relay contacts are used to control the heating element and normally open contacts are used so that the element is switched on when the relay is energised.

With the element switched on, the environment around Th1 will increase in temperature and will take Th1 higher in temperature as it does so. This causes the voltage at the input of inverter 1 to rise, and results a much larger reduction in the output voltage of this inverter. This soon results in the Schmitt trigger returning to the low state, with Tr1, the relay, and the heating element being switched off in consequence.

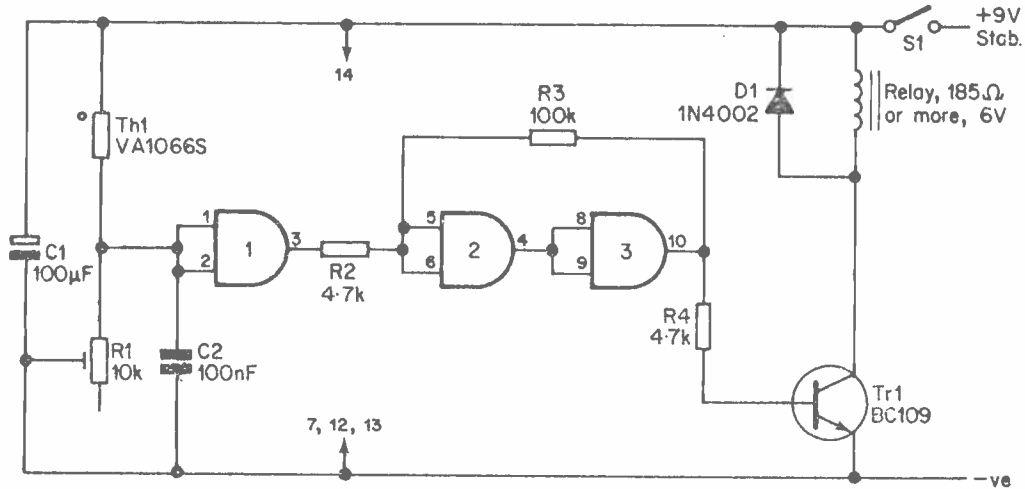


Fig. 25. A simple but high performance thermostat (about −15 to +30 degrees C.).

The temperature of Th1 and its environment then begins to fall, the voltage at inverter 1 output rises and switches the Schmitt trigger back to the high output state. The heating element is switched on and begins to heat up Th1 once again. The circuit continuously cycles in this manner and maintains the temperature of Th1 and its environment at a fairly steady level.

At first sight it may seem to be unnecessary to use the amplifier stage between the sensor circuit and the Schmitt trigger. Admittedly, the same basic circuit action could be obtained by transposing Th1 and R1, and feeding their output direct to the trigger circuit. However, the hysteresis of the trigger circuit would produce a rather wide difference between the two temperatures at which the heating element is switched on and off. This would result in the temperature being maintained only to within rather broad limits.

The circuit values have been chosen to produce only a modest amount of hysteresis so that the circuit is stable and not prone to relay chatter, and also provides a reliable and swift trigger action. The output from the sensor circuit is amplified so that a small change in the temperature of Th1 produces a large voltage change at the input of the trigger circuit, and what hysteresis there is produces only a very minor degradation in performance. C2 aids the stability of the circuit.

The circuit can be adjusted over a wide operating temperature range of about −15 to +30 degrees Centigrade. It should be possible to obtain a temperature stability of less than plus and minus 0.5 degrees Centigrade, but the accuracy obtained depends to a large extent on how good (or otherwise) Th1 is in contact with its environment.

If Th1 is to be immersed in liquids it will be necessary to mount it in a waterproof housing of some kind, such as a glass test tube or a small plastic container. Some silicon grease or a silicon grease substitute can be used to fill the container around the thermistor and ensure a good thermal contact between the thermistor and the outside surface of the container.

For optimum accuracy a stabilised supply should be used to power the circuit. As the circuit covers a very wide temperature range it is advisable to use a multiturn trimpot in the R1 position in order to make accurate adjustment of the unit reasonably easy. Alternatively, a lower value preset, say about 220 ohms in value, can be added in series with R1 to provide a fine adjustment control.

In order to set R1 correctly, Th1 should be placed in an environment which is at the desired thermostat temperature, and allowed to assume the same temperature as this environment. R1 is then carefully adjusted for the lowest resistance setting that causes the relay to be in the off position. Make sure that the relay is rated to handle the load currents and voltages concerned, as many relays are not able to control even fairly small heating elements.

Alternative Version

If the thermostat is needed for use in conjunction with a refrigeration unit the slightly modified sensor circuit shown in Fig. 26 can be used. The modification simply consists of transposing R1 and Th1 so that a rise in temperature causes the relay to be energised, and a fall in temperature causes it to be switched off.

Switch Off Reminder

It is very easy to inadvertently leave certain types of electronic equipment switched on after they have been in use. Items such as battery powered signal generators, for example, usually have no form of pilot light, and produce no visual or audible indication that they are operating. This can obviously lead to a rather shortened battery life with a consequently high running cost, and can also result in the inconvenience of going to use a piece of equipment only to find that it is non-operational due to it being left on and the battery running completely flat.

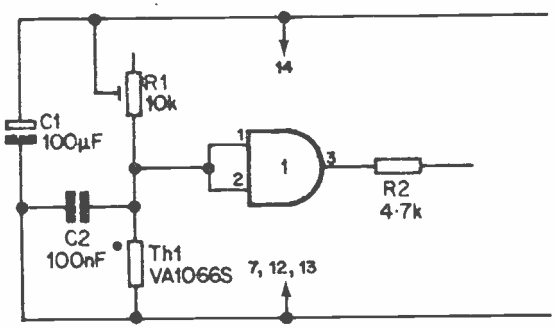


Fig. 26. Modified input stage for thermostat.

One way of overcoming this problem is to fit some kind of pilot light to such items of equipment, but to be really feasible the pilot light must have a low current consumption so that it does not greatly reduce the battery life. A popular form of pilot light for use in such circumstances is the flashing low power type, and such a design is featured in the '50 CMOS I.C. Projects' book.

An alternative form of pilot light is the type which gives a brief flash when the unit is switched off, but does not otherwise come on. This type of circuit works because switching the unit off has a positive rather than a negative (and apparently non-existent) result. There is also the novelty value of the circuit which helps to remind one to switch the unit off. Of course, the main attraction of this type of circuit over the alternative methods is that it consumes no significant power whatever.

The circuit diagram of a simple switch off reminder pilot light is given in Fig. 27, and this is extremely simple, being based on a single CMOS inverter and using very few discrete components.

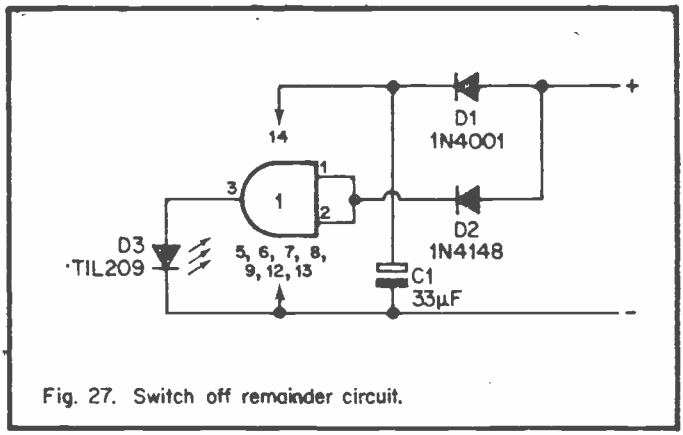


Fig. 27. Switch off remainder circuit.

C1 will quickly charge up through D1 when power is first applied to the circuit, and so power will be applied to the gate. The input of the inverter is connected to the positive supply via D2, and so the input will be at logic 1. D2 is merely used to ensure that the input is not taken higher in voltage than the positive supply to the inverter.

When the main circuit is switched off and power is also removed from the pilot light circuit, the input of the inverter will go to logic level 0. However, power will still be applied to the inverter as C1 cannot discharge into the main circuit as the necessary current flow is blocked by D1.

With the input of the inverter low, the output will go from its previous low state to the high state, and C1 will discharge through the output circuitry of the inverter an L.E.D. indicator D3. The pulse of current through D3 causes it to briefly light up and produce the required switch off flash.

2-Station Quiz Detector

A simple two station switch precedence indicator circuit was provided in the '50 CMOS I.C. Projects' book. This type of

circuit is designed to show which of two switches was operated first, and each switch operates an indicator light. When a switch is operated it causes its particular light to switch on, and blocks the other switch from turning on its indicator light. This is the sort of circuit that is used in T.V. type quizzes where the first person to press his or her switch has the first opportunity to answer the question. The circuit eliminates any arguments about who was first to operate their switch.

The circuit in the '50 CMOS I.C. Projects' book is based on a bistable multivibrator. An alternative approach is to use logic gates as such, and this system has the advantage of being able to operate with more than two switches/lights.

Fig.28a shows the circuit diagram of a two station quiz monitor circuit that is based on a couple of two input NOR gates. This circuit is only suitable for use with the 4001 device.

With neither of the push button switches operated, R1 and R3 will take one input of each gate to logic 1. The output of a two input NOR gate will be high unless one or both of the inputs are high. Since one input of each gate will in fact be high, both outputs will be low. The upper input of gate 1 is taken to the output of gate 2, and so it will be in the low state. Similarly, the upper input of gate 2 is taken to the output of gate 1, and will also be in the low state.

If, for example, PB1 is operated, the lower input of gate 1 will be taken the logic 0 and both inputs of this gate will then be at logic 0. With neither of its inputs at logic 1 the output of gate 1 will go high and D1 will light up as it will be fed with a current through R2. When the output of gate 1 goes to logic 1 it takes the upper input of gate 2 to the same logic state. If PB2 is now operated it will take the lower input of gate 2 low, but the output will still be at logic 0 as the other input will be high. Therefore, PB2 will be prevented from causing D2 to light up.

Of course, if it is PB2 that is operated first, then both inputs of gate 2 will be low, the output will go high, and D2 will switch

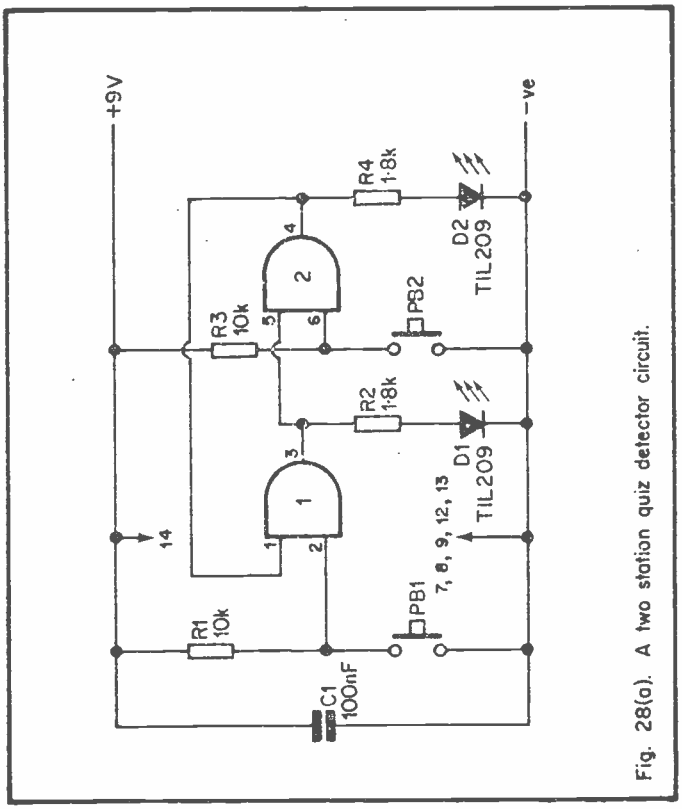


Fig. 28(a). A two station quiz detector circuit.

on. The output of gate 2 will take the upper input of gate 1 high, and operating PB1 will have no effect. The required blocking action is thus provided.

3-Station Quiz Monitor

This general system outlined above can easily be adopted for a greater number of switches by using gates having more than two inputs. The gates must have an input for each switch used, and there must be a gate for each switch. A three station circuit therefore requires three 3-input NOR gates, a four

station circuit required four 4-input NOR gates, and so on. Fig. 28(b) shows the circuit of a three station quiz monitor using a 4025 triple 3-input NOR gate.

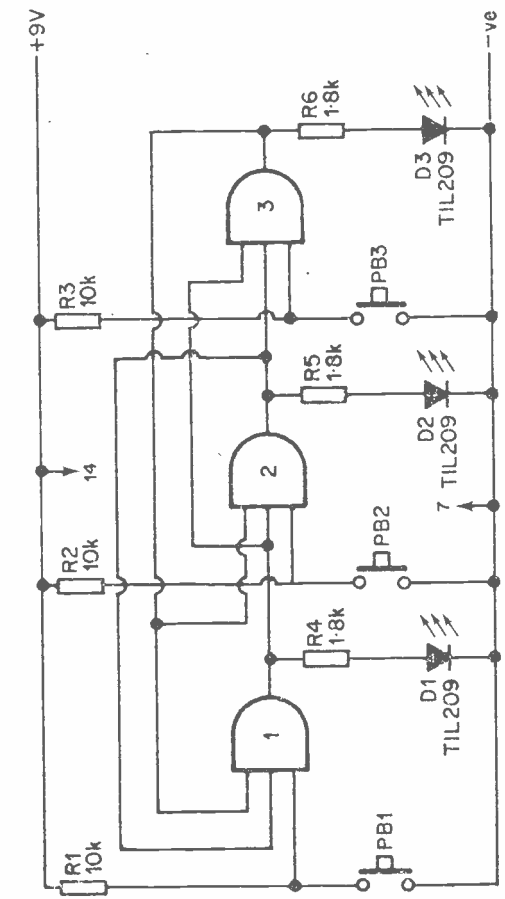


Fig. 28(b). A three station quiz detector circuit (I.C. is 4025 type).

If any input of a NOR gate is taken high, the output will be at logic 0. In other words, if input 1, *or* input 2, *or* input 3 is positive the output will be negative. It is from this that the term 'NOR' is derived.

Each gate has one input taken to logic 1 by a resistor (R1 to R3) and each of these inputs has a push button switch which when operated takes the appropriate input to logic 0. The remaining inputs of each gate go one to each output of the other gates. A L.E.D. indicator circuit is driven from the output of each gate.

Under quiescent conditions each gate has an input at logic 1, and all the outputs are at logic 0. All the L.E.D.s are therefore switched off. If a push button switch is operated, all the inputs of that particular gate will be low and the output will go to logic 1. The L.E.D. driven from the output of that gate will then light up. When the output goes to logic 1 it takes an input of each of the other gates high, and renders their push button switches inoperative.

The author has not tested a circuit of this type having four stations and using two 4002 dual 4-input NOR gates, but there is no reason in theory why such a circuit should not function perfectly well. It should be possible to expand the system to more than four stations, but in practice such a circuit would probably be rather difficult to construct, and there are probably more satisfactory ways of producing the necessary circuit action.

If desired, touch switch operation can be provided by replacing the push button switches with pairs of touch contacts and raising the value of the 10 k input feed resistors to about 10 Meg. ohms. Unless the leads between the touch contacts and the main circuitry are kept fairly short, it will probably be necessary to use screened leads here (the outer braiding connecting to the negative supply rail). Otherwise it is likely that stray pick-up in the connecting leads will prevent the circuit from functioning correctly.

Chapter 4

SPECIAL DEVICES

Like any family of logic I.C.s, the CMOS range is not merely limited to simple gate and inverter devices. There is a very wide range of more specialised and complicated CMOS I.C.s, and this final chapter will describe a number of projects based on some of these devices.

Model Traffic Light

The CMOS 4022 device is an octal divider/counter and one of eight decoder. Apart from use in applications where a divide by eight action is required, the one of eight decoder section enables the unit to be used in various multiplexing and similar applications.

The one of eight decoder consists basically of eight outputs designated 0 to 7. At the beginning of a count cycle, output 0 will be at logic 1 and the other seven inputs will be low. If an input pulse is fed to the input, the 0 output will go to logic 0 and the 1 output will go high. The next input pulse will send output 1 low and output 2 high. On subsequent input pulses outputs 3 to 7 will go high in sequence, each output only remaining at logic level 1 for one input cycle.

One possible use for the 4022 is shown in Fig. 29 which is the circuit diagram for a model traffic light control system. This could be used in various types of model layout and also makes a good demonstration logic circuit.

The circuit drives three L.E.D.s, one green, one amber (or yellow), and one red, in the correct sequence to produce a traffic light action. In other words, the green L.E.D. is switched on for a period of time, then the amber L.E.D. is switched on for a slightly shorter period of time, after that the red L.E.D. is switched on for the same duration as the green

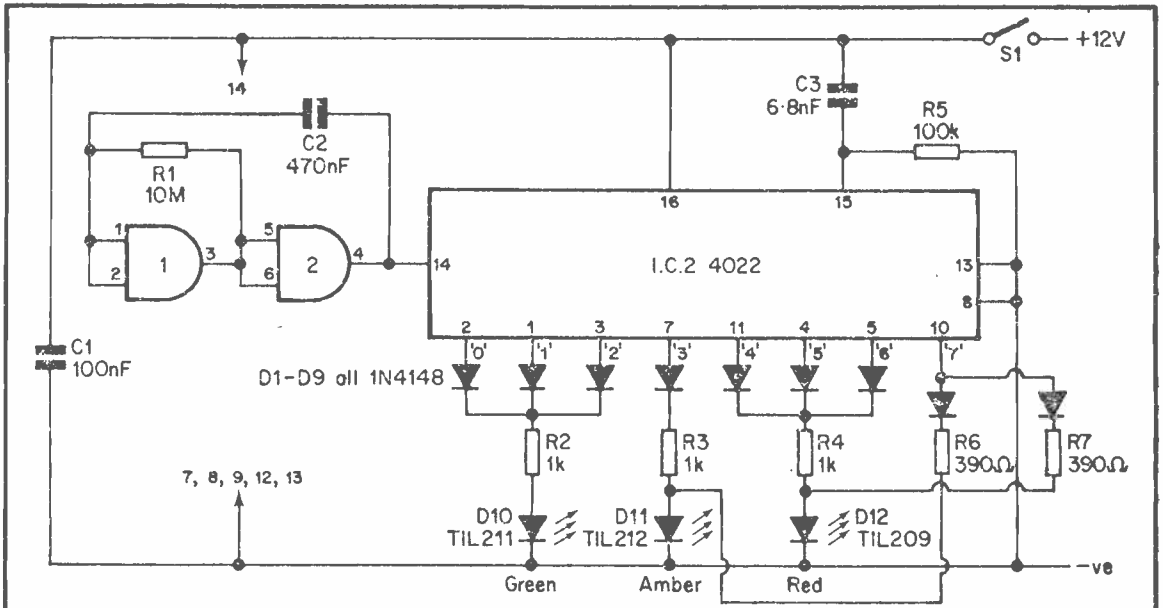


Fig. 29. A model traffic light using the 4022 as a driver/decoder (one section).

L.E.D., and finally both the red and amber lights are switched on for the shorter period of time. The L.E.D.s continuously cycle through this sequence.

When power is initially applied to the circuit a short positive pulse is applied to the reset terminal of the 4022 (pin 15) by C3 and R5. This resets the circuit to zero, and the 0 output (pin 2) goes high. The green L.E.D., D10, will be supplied with a current from the 0 output through D1 and R2, and so it will light up.

Two inverters are connected to form a low frequency (about 0.16 Hz) astable multivibrator, and this feeds the clock input (pin 14) of the 4022. The first two positive input pulses from the clock generator cause output 1 and then output 2 to go high, and these supply current to D10 via D2 and D3 respectively. On the next positive input pulse output 3 goes high and drives on the amber L.E.D., D11, by way of D4 and R3. On the next three cycles outputs 4, 5 and 6 go high, and drive the red L.E.D. on via D5, D6 and D7 respectively. On the next clock cycle output 7 goes high and powers both the amber and red L.E.D.s via D8 plus R6, and D9 plus R7 respectively. On the next clock cycle, output 0 goes high and the sequence commences once again from the beginning.

D1 to D9 are steering diodes and these ensure that the output current from whichever output is high is channelled through the appropriate L.E.D., and not into one of the other seven outputs of the 4022. Output seven has to drive two L.E.D.s whereas the other outputs only drive a single L.E.D. The two current limiting resistors associated with output 7 therefore have lower values than the current limiting resistors for the other outputs in order to provide a more consistent light output level from the L.E.D.s.

Of course, if desired, the speed at which the circuit runs through the sequence can be raised or lowered by decreasing or increasing the value of C2.

For a set of traffic lights at a cross roads an additional circuit

is required, as while the traffic on one road has a green light, the traffic on the other road has a red light. While one set of traffic has an amber light, the other has a red and amber signal. In other words, the two traffic lights run through the same sequence, but are in antiphase.

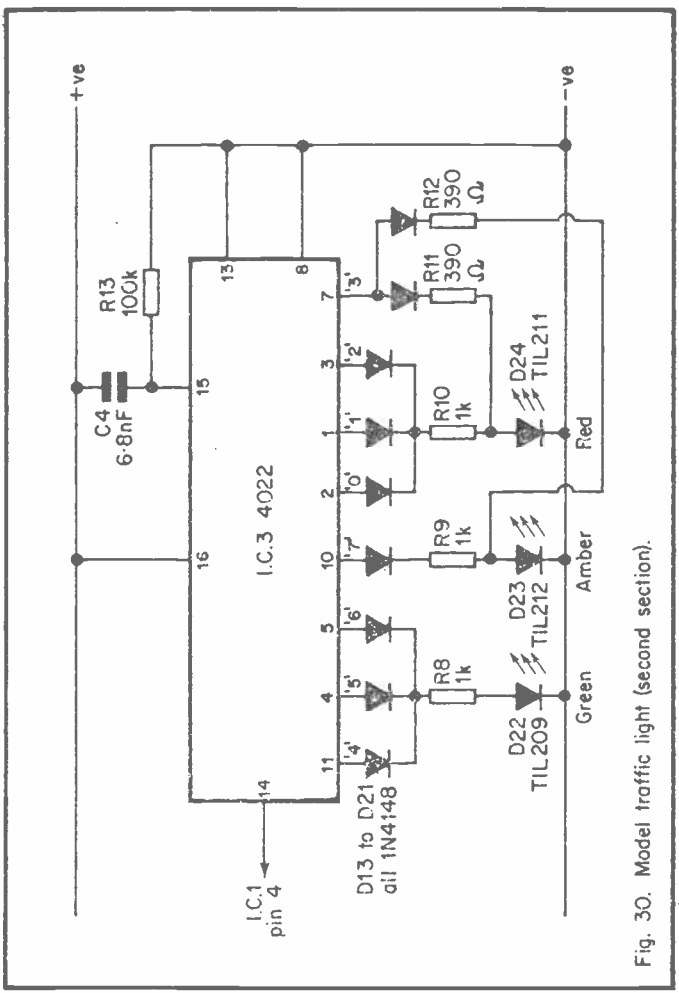


Fig. 30. Model traffic light (second section).

Fig. 30 shows the circuit diagram of a simple traffic light controller circuit which can be used in conjunction with the circuit of Fig. 29 to produce a two-directional system. The decoder/driver circuitry is basically identical to that used in Fig. 29, but while the red L.E.D. of Fig. 29 is driven from outputs 4 to 6, the red L.E.D. here is driven from outputs 0 to 2. The green L.E.D. is driven from outputs 4 to 6 instead of outputs 0 to 2. The amber and red plus amber signals are similarly transposed. Both decoder/driver circuits will be set to zero when the circuit is switched on, and they are driven from a common clock generator. They will therefore run in the required antiphase manner.

Simple Die

Many electronic die circuits have been published, and some designs are quite complex. This is not the case with the simple CMOS die circuit of Fig. 31 which must be one of the least complicated die circuits yet published.

Two inverters are connected to form an astable clock generator circuit which runs continuously while the supply is connected. The operating frequency is something in the region of 800 Hz, but the exact frequency is not important, provided it is reasonably high.

Pin 13 of the 4022, the clock inhibit terminal, is normally taken to logic 1 by R2 and the circuit is prevented from operating. However, if PB1 is depressed, the clock inhibit input of I.C.2 will be taken to logic level 0 and the circuit will begin to operate.

Outputs 0 to 5 of the 4022 are used to drive a line of six L.E.D.s, and these are numbered 1 to 6. They represent the six numbers of a die, of course. When PB1 is closed and the 4022 is operating, each of these L.E.D.s will be switched on in sequence. Then output 6 will go high, and as this is connected to the reset terminal (pin 15), the counter is immediately reset to zero by this output. Thus, output 7

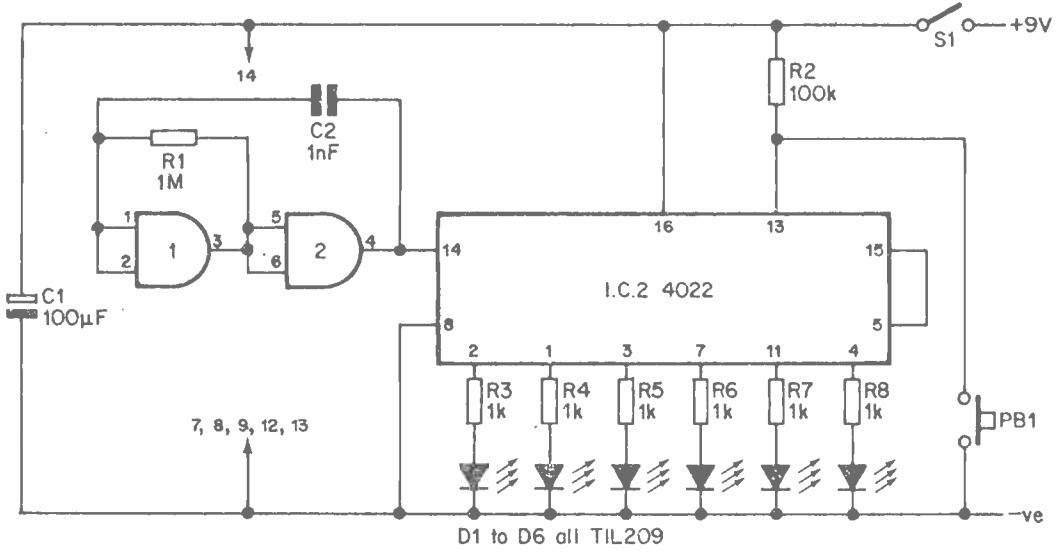


Fig. 31. A simple CMOS die circuit.

never goes to logic 1, and output 6 cannot exist at logic level 1 since the circuit is reset to zero the instant this output goes high. One of the six L.E.D.s must be switched on when PB1 is opened and the counter is halted, and it is purely a matter of chance which particular one it is. The circuit operates far too fast for the user to be able to open PB1 while a particular L.E.D. is on. In fact while PB1 is depressed, all six L.E.D.s appear to be continuously alight at reduced brilliance. The circuit therefore produces a number in the range 1 to 6 purely at random when PB1 is released after having been briefly depressed. The action of the circuit is thus a good simulation of an ordinary die.

Alternative Display

Although the circuit of Fig. 31 has the advantage of extreme simplicity, it has the disadvantage of a rather primitive form of display. A better type of display would be seven L.E.D.s in an H configuration, as shown in Fig. 32(a). This can display the numbers as they would appear on an ordinary die.

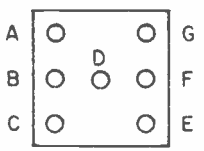


Fig. 32(a). The layout of the seven L.E.D.s of the die display.

The circuit of Fig. 31 can be made to drive this type of display by replacing the six L.E.D.s and their series resistors with a suitable gating circuit. Such a circuit could be formed from CMOS gates, but it is probably cheaper and easier to use a simple discrete gating circuit, such as that shown in Fig. 32(b).

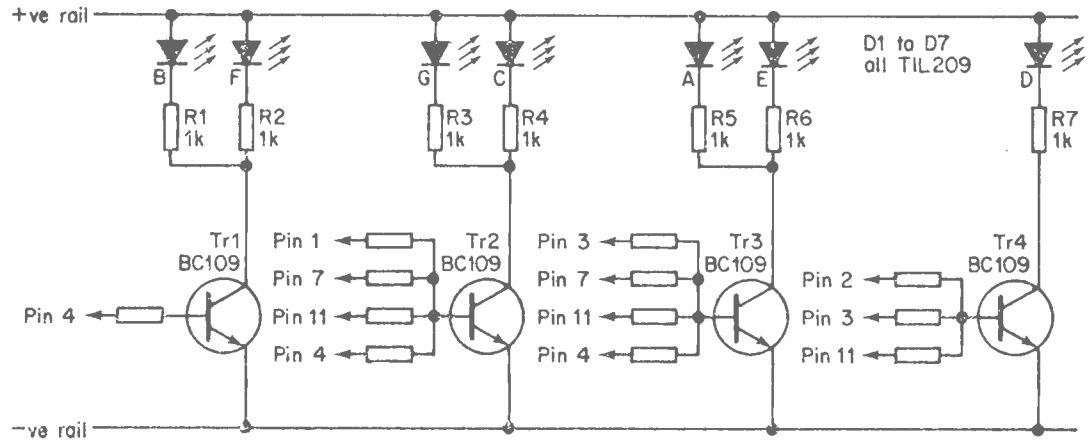


Fig. 32(b). An alternative L.E.D. display and driver circuit for the circuit of Fig. 31.

The gating circuit must drive the appropriate L.E.D.s when each output goes high. When I.C.2 pin 2 goes high, only Tr4 will be switched on and only L.E.D. 'D' will come on. A one will be displayed. When pin 1 goes high, only Tr2 will be switched on, and a three will be displayed because L.E.D.s 'A', 'E' and 'D' will come on. When pin 7 goes high it switches on Tr2 and Tr3, and produces a four display because L.E.D.s 'G', 'C', 'A' and 'E' all turn on.

As should by now be apparent, pin 11 will drive on transistor Tr2, Tr3 and Tr4, and so will switch on L.E.D.s 'G', 'C', 'A', 'E' and 'D'. Pin 4 will switch on all the transistors and L.E.D.s except TR1 and L.E.D. 'D' when it goes to the high logic state. In this way the gating circuit drives the appropriate combination of L.E.D.s from each output of the counter I.C.

Reaction Timer

Fig. 33 shows the circuit diagram of a simple reaction timing game employing the 4022 as a simple counter. This circuit is only intended for amusement purposes, and it can provide a great deal of fun. The time scale is quite arbitrary, and is merely intended to give a rough comparison of the reaction speeds of two or more players.

When S1 is switched to the 'on' position, power is applied to the circuit and C4 plus R15 set the counter to zero. D1 is driven from the 0 output of I.C.2 and this L.E.D. will therefore light up.

Inverters 3 and 4 are connected to form a simple low frequency astable clock generator having a nominal frequency of a little over 10 Hz, but R5 permits quite a large variation in the clock frequency. The counter circuit will not operate at first because inverters 1 and 2 are connected to form a Schmitt trigger circuit, and the high output of this is coupled to the clock inhibit input of I.C.2 through R3.

The output of the Schmitt trigger will only remain in the high

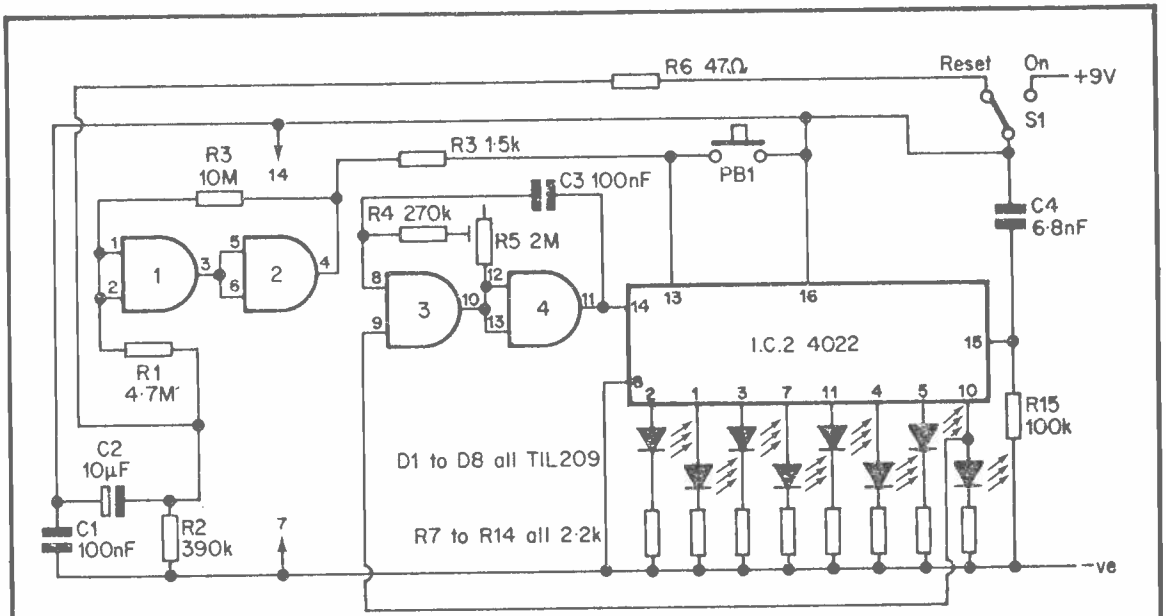


Fig. 33. Simple reaction timer game (4001 only).

state for a few seconds as C2 will charge up through R2 and eventually take the input of the trigger low. The output then goes to logic 0, and the counter circuit begins to operate. The eight outputs of the counter are used to drive a line of eight L.E.D.s, and the clock generator causes each L.E.D. in the line to be briefly strobed on in sequence. After something less than a second the last L.E.D. in the line will be switched on. When this happens, not only does the last output of the counter (pin 10) go to logic 1, but so also does the lower input of inverter 3, to which it is connected. As we have seen in previous designs, with one input of a NOR gate in a low state, the device will still act as an inverter as far as inputs to the other input terminal are concerned. If the control input is taken high though, the output will go low and signals applied to the other input terminal will have no effect.

The lower input of inverter 3 will normally be low and the astable will operate normally, but when the last output goes to logic 1 the astable will be blocked, and its output go to logic 0. This prevents the counter from continuously cycling until PB1 is depressed, taking the clock inhibit input of the counter high and stopping the count wherever it rested at the instant the contacts of PB1 closed. The continuous cycling would be undesirable as it could lead to cheating and/or arguments.

The game is very straightforward to use. S1 is set to the 'on' position and the player waits for the light to start to move down the row of L.E.D.s, as it were. The idea of the game is to press PB1 as quickly as possible when the light starts to move along the display, a rough indication of the reaction time being given by how far down the row the light gets before PB1 is operated. PB1 is then released and S1 is switched to the reset position (discharging timing capacitor C2 through current limiting resistor R6). The unit is then ready for the next round to be played.

Initially R5 is adjusted so that its slider is at about the centre of its track. If the game proves to be too easy with PB1 always being closed with the count at no more than about four, adjust R5 for a slightly lower resistance so as to increase

the clock frequency. If, on the other hand, the game proves to be too difficult with the last L.E.D. in the display often coming on before PB1 is closed, set R5 for a slightly higher resistance in order to slow up the clock oscillator slightly.

Precision Long Timer

Timer circuits of various types are very popular and are a feature of many books and magazines for the amateur electronics enthusiast. A couple of timer circuits are featured in the '50 CMOS I.C. Projects' book, and in common with the majority of timer designs these use an R – C timing network with the timing period of the unit being determined by how long it takes the capacitor to charge through the resistor to a certain voltage. Such times provide a reasonable level of performance and are generally extremely simple. However, they are rarely capable of providing a really high degree of accuracy and repeatability.

The limiting factor on the level of performance obtained is the stability and reliability of the timing capacitor used. This is often of the electrolytic type as quite high C – R values are needed in order to produce timing periods of even just a few seconds. Unfortunately, electrolytic capacitors normally have high tolerances, and inconsistent leakage resistances, and comparatively poor stability. This obviously gives considerably less than the ultimate in accuracy, and if a poor quality electrolytic is used it is likely that the circuit will fail to operate at all.

A system often used in digital frequency meters and similar items of equipment where an extremely accurate pulse length is required is to derive it from a high frequency crystal oscillator and divider chain. This system is too costly and inflexible for general purpose use, but the basically similar system of using a C – R oscillator driving a divider chain provides good performance, versatility, and reasonably low cost and complexity.

The circuit diagram of a simple timer of this type is shown in Fig. 34. Two inverters are used in the astable mode to produce a clock signal for a 4020 14-stage binary counter. The latter has outputs available from stages one, and four to fourteen. Only the output from the final stage is used in this application, and the circuit therefore divides by 16,384.

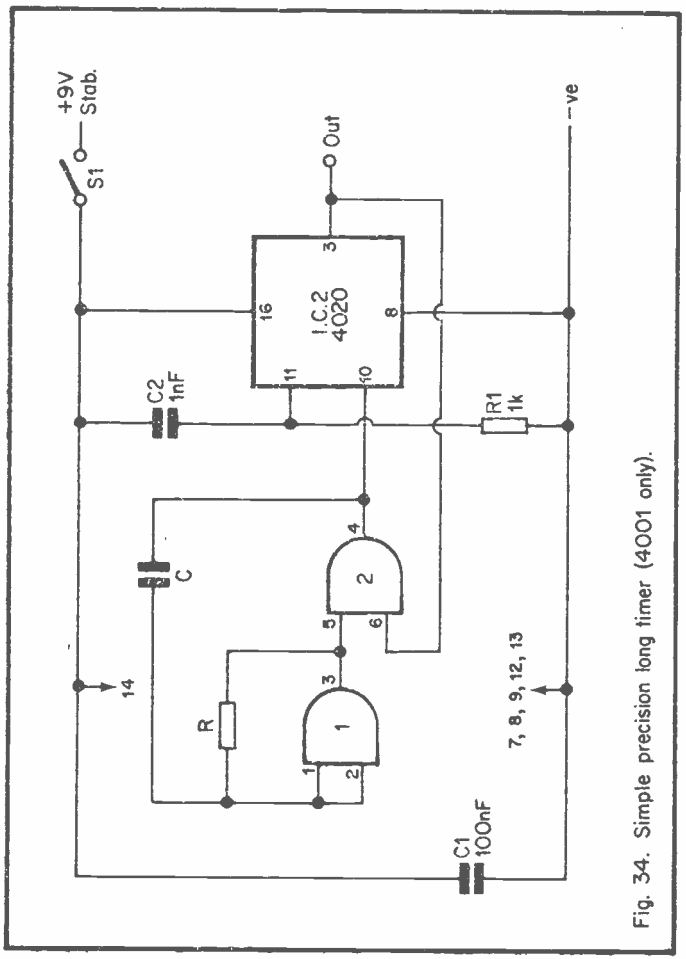


Fig. 34. Simple precision long timer (4001 only).

The circuit is designed to have an output which is normally low, and which goes to logic 1 some predetermined time after the unit is switched on.

At switch on the 4020 is reset to zero by the positive pulse generated by C2 and R1. The output is therefore low, and so the lower input of inverter 2 will also be at logic 0. The clock astable will be able to function and feed the counter with an input signal.

If the circuit was allowed to freely cycle indefinitely, the output from the unit would be a symmetrical squarewave having a frequency equal to the clock frequency divided by 16,384. However, a single output pulse is all that is required, and this is the reason for coupling the lower input of inverter 2 to the output of the counter circuit. After 8,192 clock cycles the output of the counter will go high and will take the lower input of inverter 2 high. This blocks the operation of the astable, and the output latches in the high state.

As inverter 2 is used as a NOR gate rather than a simple inverter, only a 4001 device should be employed in this circuit. The length of the output pulse is approximately equal to 12,000 C. R., and so a timing resistor and capacitor of only 100 k and 100 nF respectively will produce an output pulse of about 2 minutes in duration, for example. This enables quite long timing periods to be obtained without using an electrolytic timing capacitor.

If an output which is normally high and goes to logic 0 at the end of the timing period is required, this can be accomplished by using one of the spare inverters of the 4001 as a buffer at the output. Methods of controlling relays, L.E.D.s, tone generators, etc. from CMOS outputs have been described in previous circuits in this book.

Improved Version

One problem with the circuit of Fig. 34 is that for optimum

accuracy it must be operated from a regulated supply as the frequency of the simple clock oscillator changes significantly with variations in supply voltage (by approximately 5% per volt). The clock frequency is also largely dependent upon the characteristics of the particular gates used, and this gives comparatively poor predictability of the output pulse length.

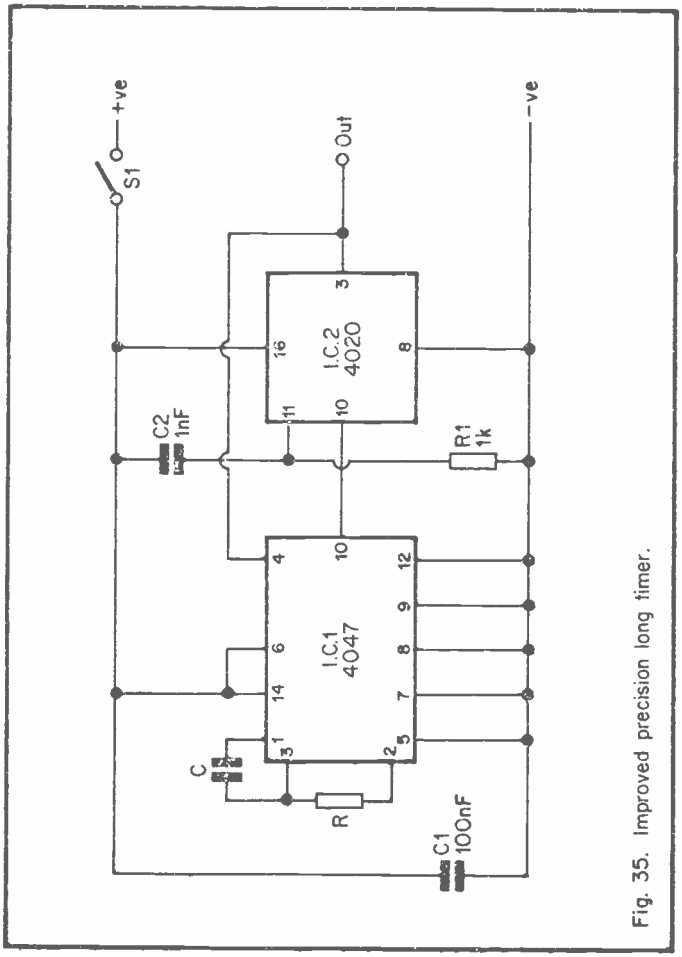


Fig. 35. Improved precision long timer.

The circuit of Fig. 35 overcomes both these problems by using a 4047 device to generate the clock signal. This is somewhat more expensive than using an astable constructed from NOR gates, but it gives improved predictability of the output pulse length, and even quite large variations in the supply potential seem to have no significant effect on the operating frequency of the circuit.

Precision Long Monostable

For some timing applications it is necessary to have a circuit that produces an output pulse of the required length each time a push button switch is operated. The circuit diagram of a precision long timer of this type is shown in Fig. 36.

Inverters 3 and 4 are used in a bistable circuit, and R2 ensures that the input of the bistable and its output (which is also the timer output) are both initially at logic 1. As the output of the circuit goes high a reset pulse is fed to the divider circuit via C2. With the output of the circuit at logic 1, the control input of the clock generator, which is produced using gates 1 and 2, will also be at logic 1, and the astable will be disabled.

When PB1 is operated, both inputs of the bistable will be at logic 0, and so the output will go to logic 0, and due to the feedback through R3 it will latch in this state. With the output low the astable will function normally and feed a clock signal to the divider circuit. After 8,192 clock cycles the output of the divider will go to logic level 1. With one of its inputs high, the output of inverter 3 must go low. This in turn drives inverter 4 input low and its output high.

As the output of the circuit returns to the high state it supplies a reset signal to the divider circuit by way of C2. The control input of the astable is taken high and this circuit is once again disabled. The circuit is then back in its original state and is ready to produce another output pulse when PB1 is once again operated.

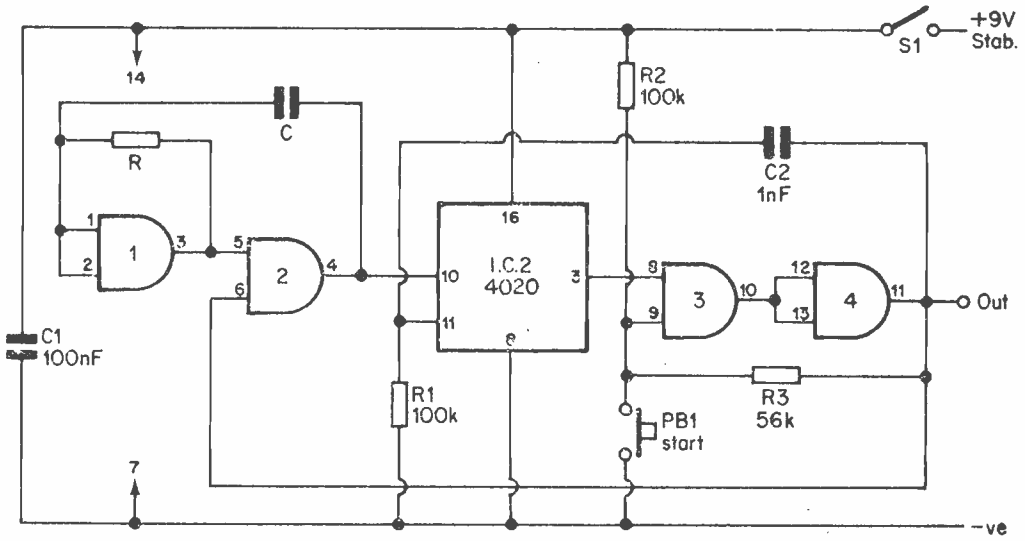


Fig. 36. Precision long timer of the monostable type.

Improved Version

The simple monostable type timer of Fig. 36 suffers from the same two drawbacks as the timer circuit of Fig. 34, and again, these can be considerably alleviated by using a 4047 device to generate the clock signal. The circuit diagram of such a unit is shown in Fig. 37.

It should be noted that when a 4047 I.C. is used to generate the clock signal the output pulse is approximately equal to 36,000 C.R. This is somewhat longer than that obtained when using an astable formed from inverters, which is of course an advantage since it enables lower C and R values to be used for a given output period.

Simple Electronic Organ

The 4047 device can be used in several astable and monostable multivibrator modes, although in many applications it can be perfectly satisfactorily replaced by NOR gates connected to produce the desired function. Due to the relatively high cost of the 4047, unless the tighter and more rigid parameters it provides are of prime importance, it is a more practical proposition to use an astable or monostable constructed from gates.

There are many applications where the use of the 4047 is justified, and an example of this is a simple electronic organ. If an astable constructed from gates was to be used as the tone generator, the output frequencies could change by more than 10% during the working life of the battery (the output from a 9-volt battery is about 9.5 volts when new and falls to about 7.5 volts when the cells are nearly exhausted). The relative pitch of the notes would remain unaltered, but if the unit was tuned to concert pitch with a fresh battery fitted, it would soon begin to drift from this pitch as the battery voltage fell. This is obviously far from ideal. Using a 4047 as the tone generator would, for all practical purposes, eliminate the drift entirely, and once tuned the unit would not need to be retuned.

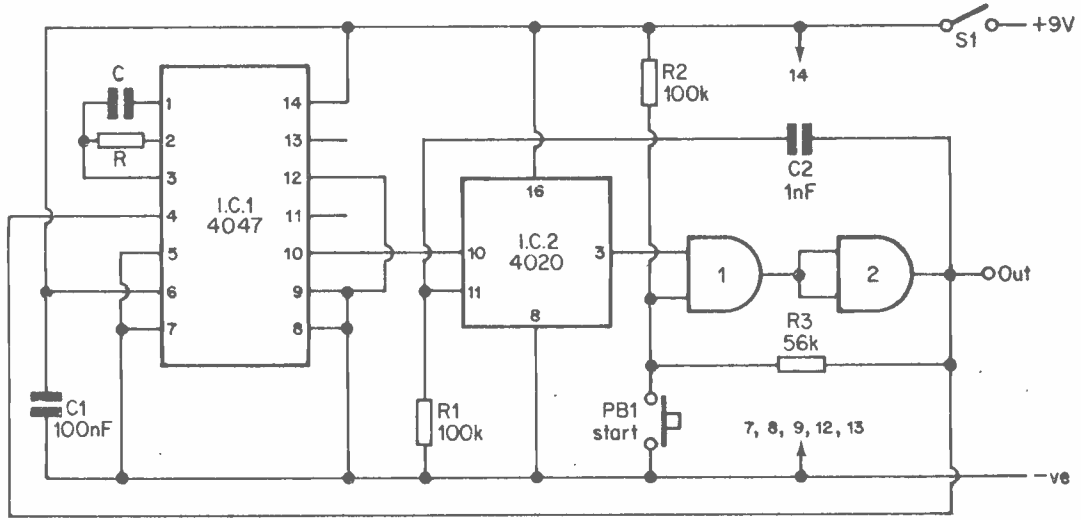


Fig. 37. Improved precision monostable long timer (4001 only).

The circuit diagram of a simple electronic organ based on a 4047 astable tone generator is given in Fig. 38. The 4047 is connected in the free running mode, but the circuit cannot oscillate until the stylus is touched onto the keyboard as there will be no timing resistance present in the circuit until this is done. C1 is the timing capacitor. R1 plus a series of 2.2 k presets form the timing resistance. The farther along the row of presets the stylus is connected the higher the timing resistance and the lower the output note. Thirteen presets are needed to provide a one octave range including the five semitones. The presets can be adjusted for a tuning range from middle C to the C an octave lower.

When used in the astable mode the 4047 has four outputs, and it is the Q output that is used here. Pin 11 is the $\overline{Q}$ (or not Q) output, and this is always at the opposite logic state to the Q output. The third output is available from pin 13, and this is at double the frequency of the Q and $\overline{Q}$ outputs. This is actually the direct output from the astable circuit and the outputs at pins 10 and 11 are obtained via a divide by two circuit and buffer stage. This is a useful feature in the present application as it enables a second octave (middle C to the C an octave higher) to be covered simply by adding a switch (S1) to enable either the output from pin 10 or that from pin 13 to be selected.

The output from the astable is fed to a simple one transistor common emitter output stage which drives a small high impedance speaker. C3 is a d.c. blocking capacitor and R2 is a current limiting resistor. R2 also forms a simple low pass filter in conjunction with C4 and this gives an improved output tone.

A piano, pitch pipes, or other source of a chromatic scale is needed in order to tune the unit. With S1 in the 'low' position, middle C is sounded on the pitch pipes or instrument, the stylus is connected to the junction of R4 and R5, and then R4 is adjusted to bring the note from the organ to the same pitch as that produced by the pitch pipes or instrument. The same basic procedure is then used for the

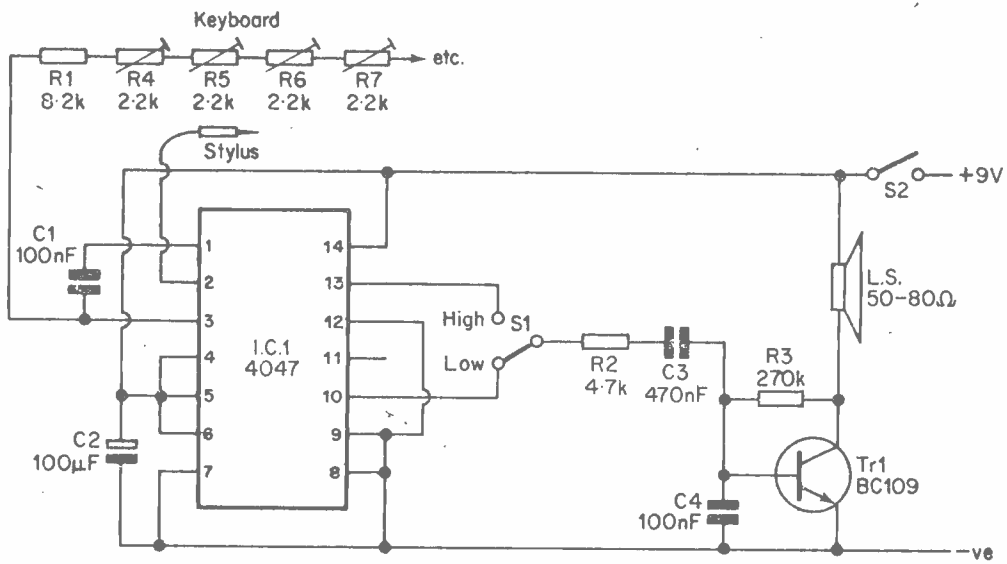


Fig. 38. A simple electronic organ incorporating a 4047 astable.

other notes working in sequence down the keyboard. The presets must be adjusted in the order R4, R5, R6, R7, etc., as apart from the final preset in the series, they all affect the tuning of more than one note. R4 for instance, is connected into circuit no matter which note is selected.

A suitable keyboard for the unit can be etched from copper laminate board, and the stylus can be an ordinary multimeter type test prod. Alternatively the keyboard can consist of a series of push button switches. Pin 2 of I.C.1 would then connect to one side of each switch, and the other connections of the switches would connect to the appropriate preset junction points.

It should perhaps be pointed out that the organ is not polyphonic, and if an attempt is made to sound more than one note, only the higher note will sound.

4047 Astables and Monostables

The 4047 is a very versatile device which can be used in three astable and three monostable modes, and basic connection details of all six modes are shown in Fig. 39.

Fig. 39(a) shows the normal method of connecting the device to produce a free running astable (there are alternative connections for this mode). The output frequency at the Q and $\overline{Q}$ outputs of a 4047 astable is approximately equal to 1/4.4 R.C. seconds with R in Meg. ohms and C in μF. The frequency at pin 13, as explained earlier, is double this frequency. R can have any value between 10 k and a few Meg. ohms, and C can have any value of 100 pF or more, but an electrolytic type cannot be used.

Figs. 39(b) and 39(c) show the methods of connecting the 4047 as a true gating and complement gating astable respectively. The true gating circuit oscillates when the input terminal is high, whereas the complement gating circuit will not oscillate unless the control input is taken to logic level 0.

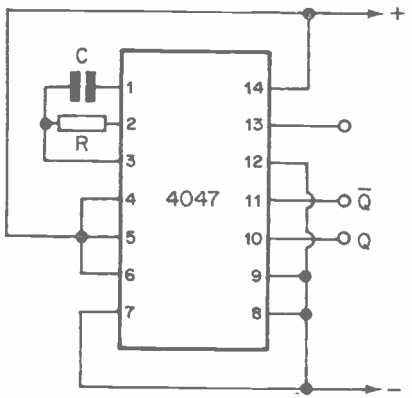


Fig. 39(a). 4047 free running astable.

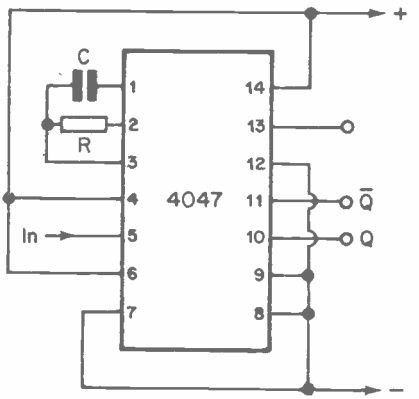


Fig. 39(b). 4047 true gating astable.

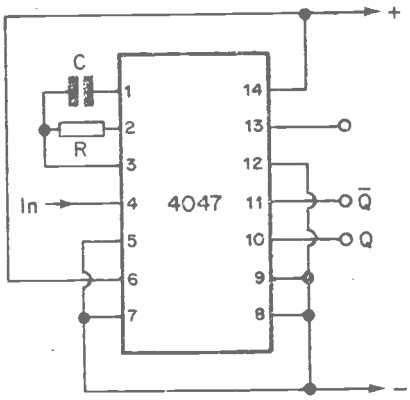


Fig. 39(c). 4047 complement gating astable.

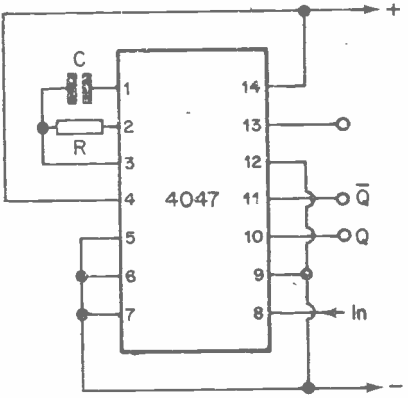


Fig. 39(d). 4047 positive triggered monostable.

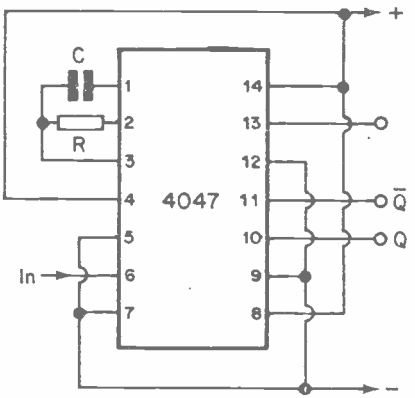


Fig. 39(e). 4047 negative triggered monostable.

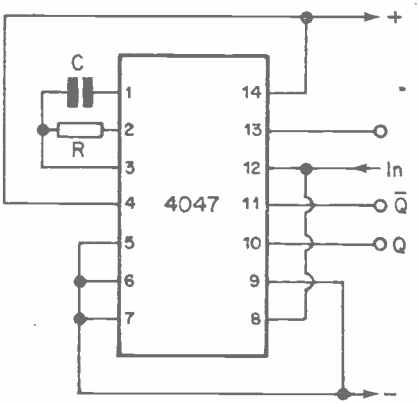


Fig. 39(f). Retriggerable 4047 monostable.

Fig. 39(d) shows the 4047 connected as a positive trigger monostable (triggered as the input goes from logic 0 to logic 1), and Fig. 39(e) shows the method of connection for a negative triggered monostable (triggered as the input goes from logic 1 to logic 0). In either case the Q output is normally low and produces a positive output pulse, and the $\overline{Q}$ output is normally high and produces a negative output pulse. The approximate duration of the output pulse is 2.48 R.C. seconds. R should be between 10 k and a few Meg. ohms in value, and C can be any value from about 1000 pF upwards. C should be a non-polarised component.

If a retriggerable monostable is required, the circuit of Fig. 39(f) can be used.

Problems can sometimes arise when a monostable having a short output pulse is manually triggered from a push button

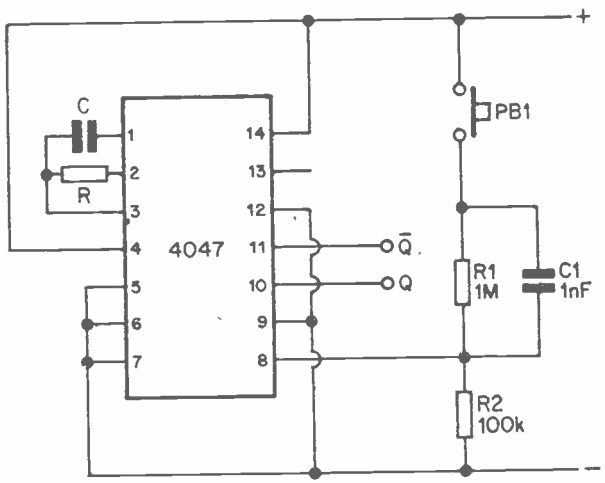


Fig. 40. Reliable method of triggering a short period monostable.

switch (or by some similar means). Mechanical switches rarely make and break cleanly, and the contact bounce that is produced can easily result in multiple operation of the monostable.

This can be overcome by using the triggering circuit of Fig. 40. When PB1 is closed, the input of the monostable is taken to logic 1, but it then quickly returns to logic 0 as C1 charges up through R2. When PB1 is released (which in practice is when any contact bounce will result in spurious triggering), the input of the monostable will remain low, and any contact bounce will be irrelevant. C1 will then discharge through R1 so that the circuit is ready to operate when PB1 is once again operated.

If a negative trigger pulse is required, R2 is connected between the input of the monostable and the positive supply, and R1, C1 and PB1 are connected between the monostable input and the negative supply.

4046 Phase Locked Loop

One of the most interesting devices in the CMOS range is the 4046 phase locked loop (P.L.L.) I.C. This device is suitable for use at frequencies up to about 500 kHz, and at any frequency of permitted supply voltage the current consumption of the unit is less than 1 mA. At audio frequencies the current consumption is only something in the region of 50 microamps.

The internal arrangement of the 4046 and basic details of the small amount of discrete circuitry required to complete a practical system using the device are shown in Fig. 41. A phase locked loop consists basically of a voltage controlled oscillator that is maintained on the same frequency and in phase with a signal applied to the input.

The voltage controlled oscillator is almost invariably of the C – R relaxation type, and the 4046 is no exception in this respect. C1 and R1 set the centre frequency of the oscillator,

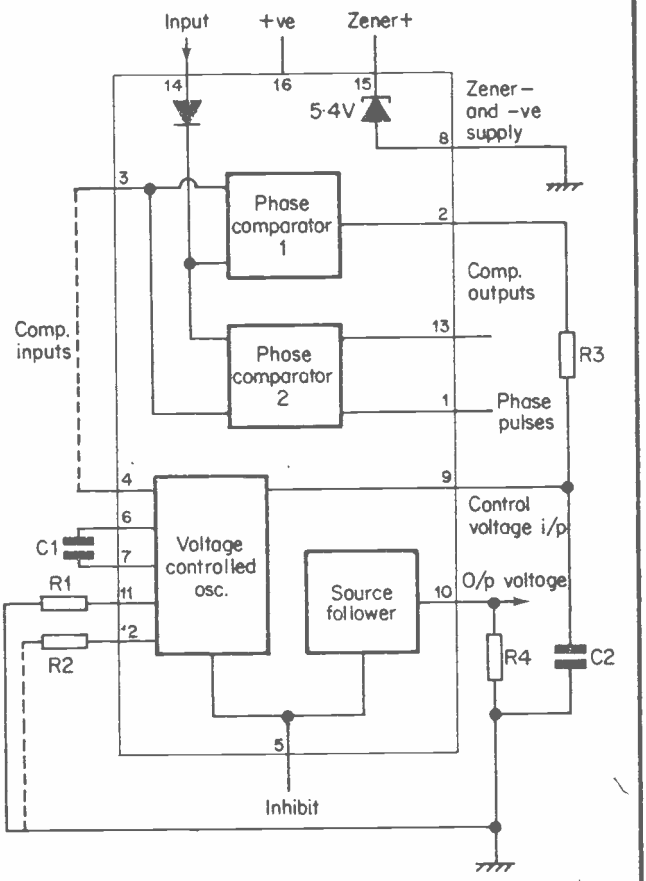


Fig. 41. The internal arrangement and simple discrete circuitry required for the 4046 Phase Locked Loop.

this being the operating frequency of the oscillator in the absence of a suitable input frequency for the unit to lock onto. R2 is only needed if it is necessary for the oscillator frequency to be offset from the centre of the circuits capture

range. The capture range is simply the range of frequencies over which the circuit can lock onto the input signal. In virtually all applications R2 will not be necessary.

The input signal is applied to one input of a phase comparator via a buffer amplifier, and the V.C.O. output is applied to the other input. There are actually two phase comparators in the 4046, and phase comparator 1 is the one which is normally used. The output from the phase comparator is a series of pulses, and these are integrated to produce a d.c. control voltage for the V.C.O. by R3 and C2.

If the input signal is somewhat higher in frequency than the V.C.O., this will cause the average output from the phase comparator to rise, and the control voltage to the V.C.O. will therefore increase. This raises the V.C.O. frequency to bring it to the same level and in phase with the input signal. Similarly, if the input frequency reduces and becomes less than that of the V.C.O., the average output potential from the phase comparator will fall and so will the V.C.O. control voltage. This causes a reduction in the V.C.O. frequency which brings it into line with that of the input signal, and also brings the two signals into phase. In this way the V.C.O. is kept on the same frequency and in phase with the input signal, but there is of course a limit to the speed at which the V.C.O. frequency can change, and if the input frequency changes too rapidly, lock will be lost. The maximum rate of change the P.L.L. can handle is known as its 'tracking rate', and is governed by the values of R3 and C2.

In most P.L.L. applications it is not the oscillator signal that is required, but the V.C.O. control voltage. P.L.L.s can, for instance, be used as f.m. demodulators in f.m. radios, wireless intercoms, and similar applications. As the f.m. carrier deviates either side of its centre frequency it produces a varying voltage at the V.C.O. input, and this signal is the demodulated audio output. In order to obtain low distortion it is necessary for there to be good linearity between the control voltage and the output frequency of the V.C.O., and P.L.L. I.C.s, including the 4046, are designed to have

good performance in this respect. Apart from use as an ordinary f.m. demodulator, P.L.L.s can also be used in various tone decoding applications, and they are indeed much used in this role.

The 4046 contains a source follower buffer stage to give a low impedance control voltage output, as the voltage a pin 9 of the device must be only very lightly loaded. R4 is the load resistor for the source follower buffer stage.

When phase comparator 2 is used, in the absence of a suitable input signal the V.C.O. frequency and control voltage fall to their minimum levels. This feature can be useful in certain applications, such as if the unit is used as a simple tone decoder which switches on some form of load in the presence of a tone which falls within the circuit's capture range.

The 4046 incorporates a 5.4 volt Zener diode, and it is a good idea to utilise this in order to obtain really good stability and reliability from the circuit.

R.C. Tone Decoder

An obvious use for the 4046 is in radio control tone decoders. The circuit diagram of a simple decoder of this type is shown in Fig. 42, and this is a basic circuit of what is often termed the 'bang – bang' type.

R1 is the load resistor for the Zener stabiliser and C1 is a supply decoupling capacitor. C2 and R2 set the V.C.O. centre frequency at about 900 Hz. The input signal is coupled to the 4046 via d.c. blocking capacitor C3, and an input signal level of at least a few hundred mV r.m.s. is preferable. R3 and C3 are the low pass filter which feeds the V.C.O. control terminal and R4 is the load resistor for the source follower output stage.

R5, R6 and R7 form a potential divider across the supply lines, and with an input frequency of about 900 Hz, the

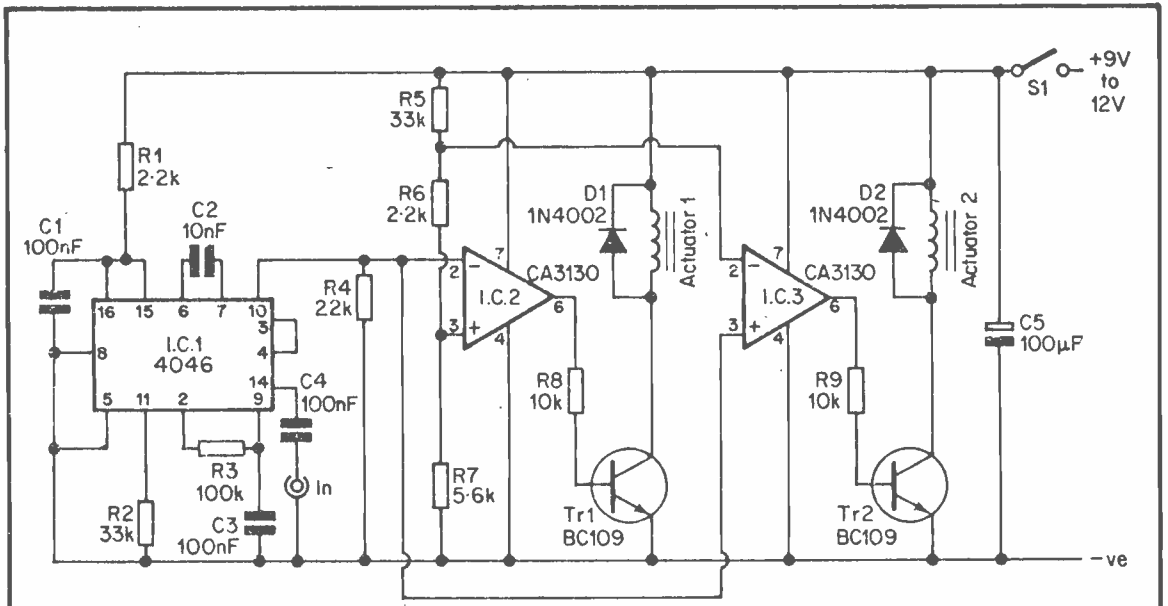


Fig. 42. An R.C. tone decoder using the 4046 P.L.L.

output voltage from I.C.1 will be somewhere between the two potentials present at the junction of R5 – R6, and R6 – R7. I.C.2 and I.C.3 are both operational amplifiers but are used here as comparators. The inverting input of I.C.2 is fed from the output of I.C.1, and the non-inverting input is fed from the junction of R6 and R7. The inverting input will therefore be at a higher voltage than the non-inverting one and the output of I.C.2 will be low. This output drives a common emitter amplifier which in turn drives an actuator. With I.C.2 output low, both these will be switched off.

I.C.3 has its inverting input fed from the junction of R5 and R6, and its non-inverting input is fed from the output of I.C.1. Like I.C.2, it will have its inverting input at a higher voltage than its non-inverting one, its output will be low, and the common emitter amplifier and actuator that are driven from its output will both be switched off.

If the input frequency to the P.L.L. is raised to about 1 kHz, the voltage at the output of the P.L.L. will rise a little above the potential at the junction of R5 and R6. The non-inverting input of I.C.3 will then be at a higher voltage than its inverting input. This will cause the output of I.C.3 to go high, the common emitter amplifier driven from its output will turn on, and actuator 2 will be supplied with power.

Taking the input frequency back to 900 Hz will cause the circuit to revert to its original condition with actuator 2 switch off again. Taking the input frequency down to about 800 Hz will result in the output voltage from I.C.1 falling below the potential present at the junction of R6 and R7. The non-inverting input of I.C.2 will then be at a higher voltage than the inverting input. In consequence, I.C.2 output goes high, Tr1 switches on, and actuator 1 is provided with power. Taking the input frequency back to 900 Hz once more causes the circuit to return to its former state with both actuators switched on.

Thus, by varying the modulation frequency at the transmitter, one or other of the actuators can be switched on, or they can

both be switched off. In a practical situation the modulation frequency would be controlled by a potentiometer. The actuators could be used to operate the rudder of a model boat, or some similar situation. Both actuators off would result in the model moving straight ahead, actuator 1 on would give steering in one direction and actuator 2 would give steering in the opposite direction.

Of course, since a variable voltage is produced at the output of I.C.1, it should be possible to use this circuitry to drive a more sophisticated output system.

Encoder

A suitable encoder for the decoder circuit of Fig. 42 is given in Fig. 43. This consists basically of a 4047 free running astable circuit with the output frequency being adjustable by means of VR1. Preset resistor R1 is adjusted to give the correct output frequency range, and in practice this is adjusted by trial and error to a setting that gives the correct action from the decoder. The output waveform of the unit is a squarewave which is rich in harmonics. This is undesirable in a modulating signal for an R.C. transmitter as it would result in a large number of spurious signals being transmitted. C3 has therefore been included in the circuit to filter out the higher frequency harmonics.

CA3130

It is perhaps worth mentioning that the CA3130 operational amplifiers used in the circuit of Fig. 42 are CMOS devices. They actually have a PMOS input stage, bipolar main amplifier stage, and a CMOS output stage. This makes the CA3130 an obvious choice when an operational amplifier for use with CMOS logic devices is necessary, since it has similar input characteristics to CMOS devices (a 1.5 million Meg. ohm input impedance for instance) and it also has the large output voltage swing associated with CMOS devices. It is capable of

operating with the inputs at voltages down to and even slightly below the negative supply rail potential. The CA3130 is capable of a 15 MHz gain bandwidth product and a slew rate of 30 volts per microsecond. It is one of the most versatile devices currently available.

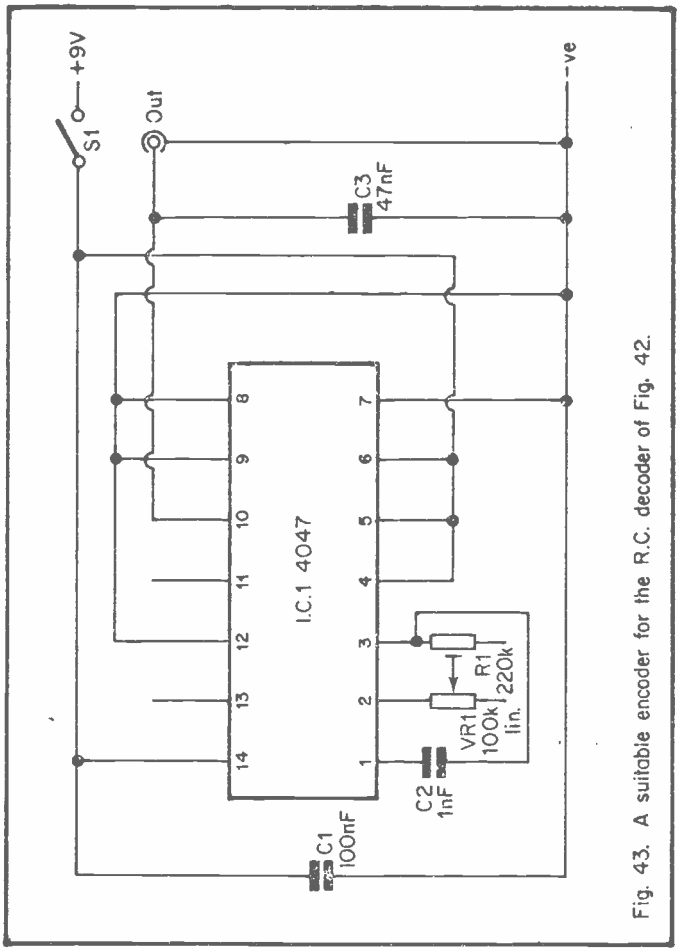


Fig. 43. A suitable encoder for the R.C. decoder of Fig. 42.

The 74C90 Device

The 74C90 I.C. is a pin for pin equivalent to the TTL 7490 device, but it has CMOS characteristics. There is in fact a range of such devices, the 74C02 device, for instance, being a CMOS quad 2 input NOR gate having the same pin function arrangement as the TTL 7402 device (and is therefore not a direct replacement for the 4001 quad 2 input NOR gate). Because the 74C** series of devices have CMOS characteristics they obviously cannot be used as direct replacements for their TTL counterparts. Neither is it always possible to use all 74C** series devices in a circuit designed to take ordinary 74** series devices and still obtain satisfactory results. CMOS devices have a far lower output current capability than TTL devices, and this will often prevent 74C** devices operating in a 74** circuit. There are one or two exceptions to this such as the 74C48 BCD to seven segment decoder which can source a current of 50 mA, but in general the 74C** I.C.s are ordinary CMOS devices.

It is perhaps worthy of mention here that most CMOS I.C.s are not capable of driving a TTL input. CMOS 4049 (inverting) and 4050 (non-inverting) hex buffers can be used to interface a CMOS output to a TTL circuit. Note that the 4049 high current buffer should not be used in linear applications, including multivibrators, timers, etc., as it might be damaged by excessive power dissipation.

The 74C90 is one of the most useful I.C.s in the 74C** series of devices. No doubt many readers will be familiar with the 7490 TTL device which is much used in decade counter circuits. An interesting feature of the 74C90 (and 7490) is that it contains separate divide by 2 and divide by 5 circuits, and it can therefore be used to provide division rates of 2, 5, or 10. Fig. 44 shows the method of connecting the 74C90 to obtain divide by two and divide by five functions. For a division rate of ten, the two dividers are connected in series. If one section is not used, connect the input to the negative supply rail.

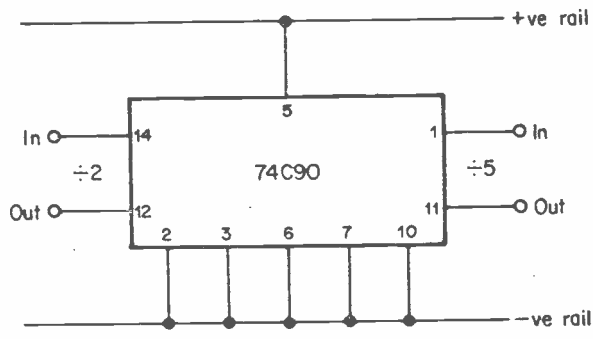


Fig. 44. The 74C90 as a divide by 2 and 5 counter.

An obvious application for the 74C90 is in a crystal calibrator of the type where a crystal oscillator generates an accurate 1MHz signal, and one or more frequency dividers are used to produce lower frequency calibration signals from the 1 MHz signal. Calibration oscillators were covered in the '50 CMOS I.C. Projects' book, and one design featured there uses a 4017 divide by ten stage to provide a 100 kHz signal from the 1 MHz oscillator.

By substituting a 74C90 divider for the 4017 divider an additional output at either 500 kHz or 200 kHz (depending upon whether the divide by two circuit or the divide by five circuit is used first in the divider chain) can be obtained. The 200 kHz output would be particularly useful as it coincides with the 200 kHz B.B.C.l.w. transmission which is used as a calibration standard for the unit. This would ensure a strong output at 200 kHz and would make it very easy to obtain a high level of signal injection into the receiver used to aid the calibration process.

Simple Timer

The divide by five ability of the 74C90 can be useful in applications where the 50 Hz mains is used to provide a 10 Hz or 1 Hz timebase signal. A simple example of a project of this type is the one second flasher/timer circuit shown in Fig. 45. Devices of this type merely provide a brief flash from a lamp at one second intervals, and are mainly used in photography, although there are no doubt other possible applications for them.

The input of the unit could be fed from a main transformer, but this is not really necessary and stray pick-up of mains hum provides a suitable input signal. The extremely high input impedances of CMOS gates makes it very easy to obtain a signal in this way, and in this case inverter 1 is used to pick-up the mains hum. D1 and D2 protect the input of inverter 1 against static voltages. As these diodes are connected back to back they will not provide a low impedance path regardless of the polarity of the input signal. Only leakage current will flow through these diodes, and such currents will only be extremely low as a silicon diode has a reverse resistance of something in the region of one thousand Meg. ohms. However, this is low enough to leak away any static charges, and is high enough to readily enable the circuit to obtain adequate signal pick-up. A length of lead or a piece of metal is needed to act as a sort of aerial to pick-up the mains signal, and probably the most practical solution here is to use the case of the unit (which should obviously be of metal or largely of metal construction).

The output from inverter 1 will contain a lot of general noise and the rise and fall times of this signal may be rather long. CMOS dividers require an input signal having a risetime of less than 5 microseconds in order to ensure correct operation. A slower risetime could easily result in a malfunction of the circuit, and so too could any noise on the input signal.

Inverters 2 and 3 are connected as a Schmitt trigger having a substantial amount of hysteresis and this provides an output

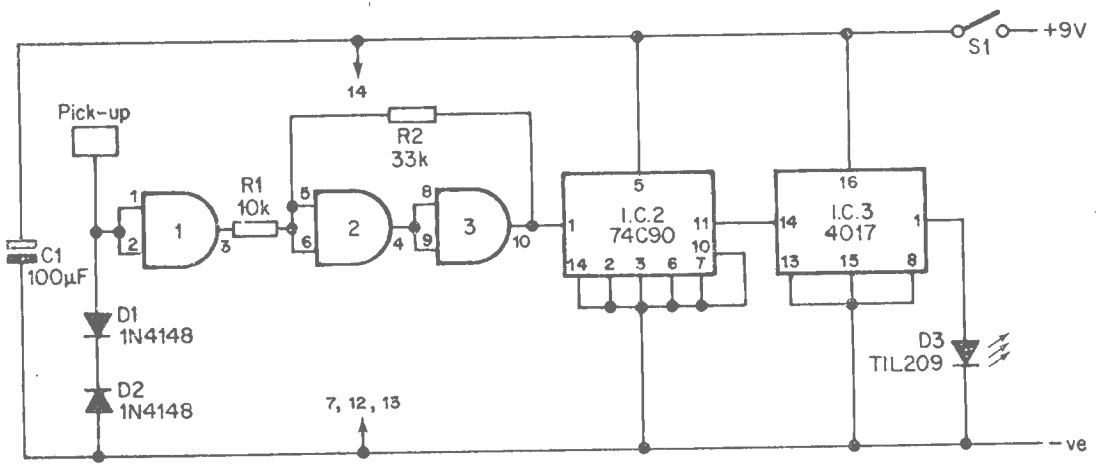


Fig. 45. A one second flasher/timer using the 50Hz mains as a timebase.

signal which has the necessary fast risetime and freedom from noise.

The 50 Hz output from the Schmitt trigger is taken to a 74C90 divide by five circuit, and the 10 Hz output from this is connected to the input of a 4017 divide by ten circuit.

The 4017 is very similar to the 4022 device covered earlier in this book, but instead of an octal divider/counter and one of eight decoder, it is a decade counter/divider and one of ten decoder. D3 is driven from one of the series of ten outputs (output 5 in fact) and so it will be switched on for a period of 100 mS at 1 second intervals.

If the unit is needed in order to provide a 1 Hz squarewave clock signal, this can be obtained from pin 12 of I.C.3, which is its carry-out terminal.

Components

The type numbers under which the CMOS I.C.s employed in the projects in this book are sold have already been discussed, and will not be repeated here. Details of the pinouts of the devices specified for the various projects are shown in Fig. 46, and this includes transistors and diodes as well as the CMOS I.C.s.

There are many substitutes for the transistors and diodes specified for the various designs, but in general the specified types are very widely available and about the cheapest suitable types.

All fixed resistors are $\frac{1}{8}$, $\frac{1}{4}$, $\frac{1}{3}$, or $\frac{1}{2}$ watt types of the usual tolerance (5% up to 1 Meg. ohm, 10% above 1 Meg. ohm). Potentiometers are all carbon types, and the circuit diagram will show whether a linear or logarithmic type should be used. Presets can be virtually any type, unless the text states otherwise, and it is simply a matter of choosing the cheapest type that will fit well into the physical layout of the unit.

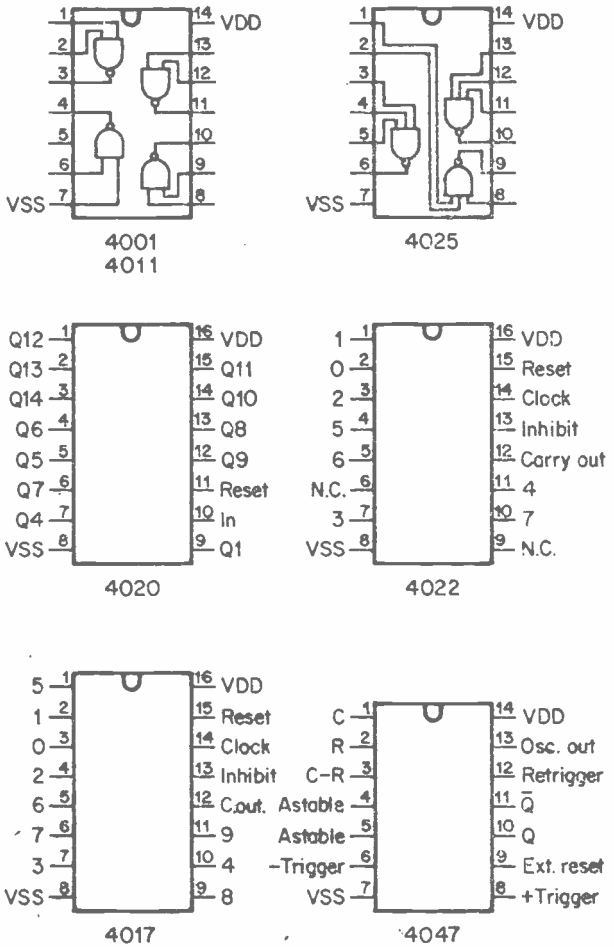
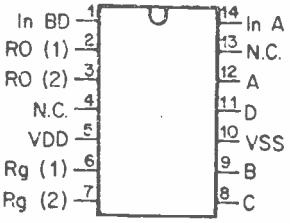
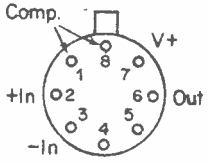


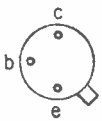
Fig. 46. Leadout and pinout details of the semiconductors employed (top views of I.C.s, base views of transistors). See Fig. 41



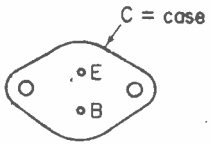
74C90



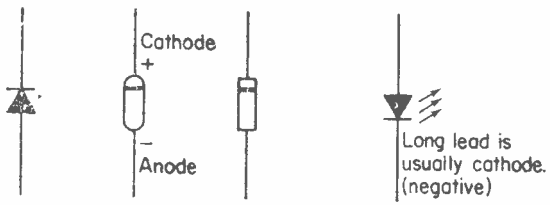
CA3130



BC109
BC179
(viewed from
underside)



BD121



OA91
1N4148

1N4001
1N4002

Zeners

LEDS
TIL209 etc.

in the projects in this book.
for 4046 details.

Non-electrolytic capacitors should be plastic foil types having a tolerance of 20% or better. If in doubt about the voltage rating of electrolytic types, choose one having a working voltage a little in excess of the supply potential used.

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Second Book of CMOS IC Projects

- Due to the fantastic success and popularity of our book No. 224 "50 CMOS IC PROJECTS" by Mr. R. A. Penfold which we produced in 1977, we have published a second book.

- Although the original book covered a very wide range of projects it by no means included all the possible uses of CMOS devices. The aim of this second book is to provide a further selection of useful circuits, mainly of a fairly simple nature, and therefore within the capabilities of both the beginner and more advanced constructor.

- The contents of the second book have been selected to produce a minimum of overlap between the two books and the versatility of CMOS devices is such that there is no problem in achieving this.

- The text is divided as follows: Chapter 1 serves as an introduction; Chapter 2 covers multivibrator projects; Chapter 3 covers amplifier, trigger and gate projects; Chapter 4 covers special devices.

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